Final Report

for the

Design and Development
of a
Non-Dissipative Charge Controller
using a
Rotary Transformer

Contract No. NAS5-9204

Prepared By

Matrix Research and Development Corporation
11 Mulberry Street Nashua, New Hampshire
03060

For

National Aeronautics and Space Administration Goddard Space Flight Center Greenbelt, Maryland 20771 SUMMARY - The purpose of this report is to discuss the design and operation of a Non-Dissipative Charge Controller using a Rotary Transformer, developed for NASA/GSFC by Matrix Research and Development Corporation, under NASA contract NAS5-9204.

The object of the contract was to design a more efficient means of utilizing output of a solar array to provide power to a spacecraft's battery and electronics. The design was to incorporate a rotary transformer to couple the power from a rotatable solar array to the spacecraft, thereby eliminating the need for slip rings.

The most significant conclusions reached during the contract are:

- 1. A rotary power transformer can be effectively integrated into a non-dissipative charge controller which maximizes the power obtainable from the solar array.
- 2. A rotary power transformer can be fabricated which is of sufficiently small size, light weight, and high efficiency as to be practical for use in spacecraft power systems.

The results obtained warrant extension of this work to increased power levels of the charge controller and transformer, and also developing a prototype system using solar cells and batteries.

Z. TABLE OF CONTENTS

Section	Descr	·ipti on	Page	e s
1	Summ	ary	i	i
2	Table	of Contents		
3	List	of Illustrations	v -	
4	List of Tables			ii
5		uction		_
6	Histor	rical Section	3 -	
	6.1	Inverter		
	6.2	Rotary Transformer		
	6.3	Pulse Width Switch	8	
	6.4	Pulse Width Control	ำ	
	6.5	Power Rectifier		12
	6.6	Maximum Power Controller	13	
		6.6.1 Power Sensor Technique		19
		6.6.2 Current Sensor Technique	· · · · · ·	
•	6.7	Trickle Charge Controller	20	
	6.8	Spacecraft Power Simulator	21	
	6.9	System Testing	22	
7	Techn		23 -	3 9
	7.1	-	26 -	27
	7.2	Pulse Width Switch and Filter		2.3
	7.3	Pulse Width Controller	3 n	
	7.4	Rectifier	31	• •
	7.5	Synchronous Detector	3.2	
	7.6	Jitter Generator	33	
	7.7	Current Sample Amplifier	3.1	
	7.8	Current Transformer	35	
	7.9	Battery Charge Detector	36 -	37
	7.10	Trickle Charge Control	3 ~	
	7.11	Constant Voltage Control	30	
. 8	Simula	tor Section	40 -	42
	8.1	Solar Array Simulator	40	
	8.2	Battery Simulator	41	
	8 .3	Spacecraft Electronics Simulator	42	
9	New T	echnology	ი 3	
10	Conclusions and Recommendations			95
11	Bibliography			
12	Glossa	ry	97 -	104

Section	Description	Pages	
	APPENDICES		
. I	Test Transformer (Rotary Transformer No. 1)	I-1 - I- 9	
II	Mathematical Transformer Model (Rotary Transformer No. 2)		
III	Redesigned Transformer (Rotary Transformer No. 3)		
IV	Maxin um Power Conditions		

3. LIST OF ILLUSTRATIONS -

Figure	Description	Page
1	Block Diagram	. 43
2	Bridge Inverter	. 44
3	Simplified Inverter and Current Feedback Drive	. 45
. 4	Pulse Width Switches	. 45
5	Preliminary P. W. Controller.	. 47
6	Synchronous Rectifier Using SCR's	• 47 • 48
7	Block Diagram	. 40 . 49
8	CHIEFERT SAFRENCE I PRINTES AND TRACE CALL	. 49
9	Current Sample Circuit - Output we Incut	. 50
10	Multiplier	. 51
11	Multiplier Multiplier Output vs Inputs	. 52
12	Synchronous Detector	. 53
13	Synchronous Detector Test Setup for Power Measurements	. 54
14	Test Panel	. 55
15	Test Panel	. 56
16	Efficiency Test Setup	. 57
	Non-Dissipative Charge Controller using a	
17	Rotary Power Transformer.	5 8
18	Inverter	59
19	Switching Regulators	60
20	Pulse Width Regulator	61
21	Synchronous Detector	62
22	Jitter Generator	6 3
23	our out outspie Minbiller	64
23 24	Battery Full Charge Detector	65
	Trickle Charge Control	6 6
25	Typical Solar Cell Curves	67
26	Solar Panel Simulator	68
27	Battery Simulator	69
28	Spacecraft Electronics Simulator	70
29	XIOZIA Transformer	71
30	XT609B Transformer	72
31	A1025 Transformer	72
32	A1030 Transformer	74
33	A 100/ Transformer	75
34	Albiy Transformer	76
35	XT596A Transformer	77

Figure	Description	Page
36	XT637 Transformer	78
37	XT638 Transformer	79
3 8	XT633 Transformer	8 ó
3 9	XT639 Rotary Transformer	81
40	XT626 Choke	32
41	XT634 Choke	93
42	XT628 Choke	84
43	XT631 Choke	8 5
44	XT635 Choke	86
45	Test Transformer	1- 5
46	Mathematical Model	
47	T: 1 T .	U-23
48		II-24
49	T	II-25
50	T	II - 26
51	117: 1: A	II-27
52		II-16
53		II-17
54		I-18
55		I-19
56		U-20
57		I-21
5 8		I-22
59	A1 '	I-23
60	70 - 11 · 70 ·	I-24
61	m m c	I-25
62	Equivalent Circuit for Maximum Power Calcula-	
	. •	T A

を なる なる 一 できる

4. LIST OF TABLES -

Number	<u>Description</u> <u>Page</u>
1	Test Data on Current Sample Circuit
2	Test Data on Multiplier
3	Maximum Power Controller Test Data -
	Manual vs Automatic Controlling
4	Maximum Power Controller Test Data -
·	Output Power vs Load
5	Final Test Data
6	Transformer Characteristics

INTRODUCTION - The purpose of this report is to discuss the design and operation of a Non-dissipative Charge Convroller using a Rotary Transformer, developed for NASA/GSFC by Matrix Research and Development Corporation under NASA Contract NAS5-9204.

The object of the contract was to design and fabricate a rotary power transformer of small size, light weight, and high efficiency, and to integrate the transformer into a charge control circuit which maximizes the power obtainable from a solar array. The rotary transformer couples power from a rotatable solar array to the spacecraft, thereby eliminating the need for slip rings.

Figure 1 is a block diagram of the general technique which was studied. An inverter is used to chop the output of the solar array to produce an alternating voltage which is transmitted to the spacecraft through a rotary transformer. The output of the rotary transformer is then rectified producing a direct voltage. This is then fed into a pulse-width regulator which transforms the supplied voltage to the level required to charge the battery. The pulse-width regulator can be considered as an adjustable DC transformer, since it can step down a direct voltage without "dissipating" power (Ein Iin Eout Iout). The pulse-width regulator can therefore be used to match the impedance of the solar array to that of the battery, providing an optimum power transfer. The constrol for the pulse-width regulator is provided by a maximum power controller which is capable of producing a control signal that causes the pulse width regulator to match the solar array impedance to the battery impedance.

Two n ethods of maximum power controlling were investigated under this contract. The first system used a power sensor which was located at the output of the rectifier. The output of the power sensor was fed into the maximum power controller which compared the phase and amplitude of the output of the power sensor to a low frequency jitter signal injected into the control loop. From this is produced the desired control signal for the pulse-width regulator.

The second system tested used a current sensor on the output of the pulse-width regulator. The output of the current sensor was fed into the same maxinum power controller as mentioned previously. However, in this case, the output current of the pulsewidth regulator was maximized instead of the power output of the rectifier.

Since the circuitry required to maximize the battery input current is less than that required to maximize power, and since maximum current into the battery is equivalent to maximum power into the battery (discussed in Appendix IV), the current maximizing circuitry was chosen for the final design.

The breadboard also includes circuitry for trickle charging the batteries. This is accomplished by means of a DC current sensor on the output of the maximum power controller which connects to the battery. The output of the DC current sensor goes to a regulator which controls the pulse-width regulator, thereby maintaining a fixed low current into the battery. Switching from the maximum power mode to the trickle charge mode is controlled by a tunnel diode level detector which connects to the third electrode of one of the battery cells.

As part of the breadboard testing program, a spacecraft power simulator was designed and constructed in order to provide realistic test conditions.

In the following text, the Charge Controller and its evolution are covered in detail. First is a discussion of the development of each major component and circuit of the system. Following this is a circuit description of the final breadboard. The next section contains a discussion of the spacecraft power simulator and a description of the testing done on the breadboard. The last section prior to the Appendices is a discussion of the recommendations and conclusions reached during the contract.

6. HISTORICAL SECTION

INVERTER - The goal of the inverter design was to produce an inverter that would operate efficiently over a wide range of input current and voltage, while adhering to the following design criteria:

- 1. The switching frequency should be higher than about 10KHz and should be stable.
- 2. It should be capable of handling voltages as high as 50DV.
- 3. It should be capable of handling steady-state input currents of 2.5 amps and transients to 5 amps.
- 4. The weight should be kept to a minimum.
- 5. Reliability should be maximized.

Two basic types of inverters were considered: a 2-transistor, center tapped circuit, and a 4-transistor bridge circuit. The advantages and disadvantages of each type are outlined below.

CENTER-TAPPED

Advantages

- 1. Higher efficiency since there is only one transistor drop.
- 2. Higher reliability due to less parts.
- 3. Less weight due to fewer parts.
- 4. Less complex drive circuitry.

Disadvantages

- 1. Higher voltage stress on the transistors.
- 2. More wire required on transformer primary.
- 3. Larger voltage spikes since the "off" side of winding is open circuited.

BRIDGE

Advantages

- 1. Transistors see lower voltages.
- 2. Less wire required on transformer primary.
- 3. Less overshoot since both ends of the primary are returned to low impedances.

Disadvantages

- 1. Lower efficiency since there are two transistor drops.
- 2. Large current spikes or voltage spikes if transistors do not switch at the proper times.
- 3. Higher weight
- 4. More complex drive circuitry.

Tests of preliminary circuits of both types show that higher efficiency could be obtained with the 2-transistor switch, however the maximum allowable collector voltage rating that could be obtained for a transistor which could meet the other requirements seemed to rule out the 2-transistor circuit. The combination of a normally higher transistor operating voltage with the 2-transistor circuit, plus the presence of higher spikes due to the positive-going end of the primary being open circuited, produced voltages considerably above the maximum collector rating of the transistors (nominally 100DV).

Attention was therefore focused on the bridge inverter. The major problem encountered with this circuit was proper timing of the switching waveforms. In the bridge circuit (Figure 2), there are two transistors in series between B+ and ground. If both these transistors were to conduct the same time, a large current surge would be drawn through them with a resulting loss in efficiency. It is therefore very important that the "on" transistor be turned "off" before the second transistor is turned "on". The problem is caused by the storage effect of the transistors, since if both the transistors are switched at the same instant, the "off" transistor

switches "on"; however, the "on" transistor remains "on" for the length of the storage time of the transistor. In order to compensate for this effect, it would be necessary to introduce some delay into the waveform which drove the transistors "on". Since the storage time of a transistor varies with the base current, this delaying circuit would have to be proportional to the driving current for best results.

With this characteristic in mind, and with the further knowledge that a bridge is somewhat less efficient due to its two series transistors, it was decided to take a further look at the 2-transistor inverter.

The further study into the 2-transistor inverter was prompted by a new line of transistors produced by "Solitron". Their 200V 10 amp switching transistors overcame the major problem confronting the 2-transistor inverter, namely transistor breakdown voltage. Also, the improved rotary transformer had less leakage inductance and therefore produced lower voltage switching spikes which also helped to solve the problem. With these developments, the 2-transistor inverter design was decided upon.

The problem of providing an efficient drive system for the inverter transistors was an area that was given considerable thought. The conventional system is to drive the transistors with windings from a magnetic oscillator. This technique requires that the drive level be set at the maximum current expected to be handled by the inverter. However, since the inverter operates over a considerable range, this means an excess drive would be supplied at anything less than the expected maximum level. Also, if due to some unforseen conditions the maximum level was higher than expected, the drive would be insufficient.

Since the best drive conditions for a saturating switch transistor is with the base current of 1/10 the collector current, some sort of current feedback from collector to base seemed to be the best solution. Figure 3 shows the technique used. The collector current in the "on" transistor supplies the base current for itself. By using one transformer for both transistors, balanced positive and negative flux levels are obtained in the transformer core, thereby requiring a smaller transformer than that which would be if a separate transformer were used for each transistor. Also, since the transformer

is driven in both directions, a low impedance negative voltage is obtained on the base of the transistor which is turning "off", thereby enhancing switching speed.

Although this circuit will free-run due to the saturation of the drive transformer once oscillations are started, it is not a self-starting configuration. Also, there will be frequency variations due to maximum flux level changes with temperature. Therefore, it is desirable to use a stable oscillator to start the circuit and to provide a stable operating frequency with temperature. This is accomplished by adding another winding to the drive transformer. This winding is driven by a magnetic oscillator. Due to the large voltage or current step-up, a low power signal into the winding is capable of initiating a state change in the inverter. Once the state change is initiated by the oscillator, the regeneration of the inverter causes rapid switching to its other state.

To further enhance switching speed and to reduce storage time, transistors were added from base to emitter on the inverter transistors. These transistors are driven by the oscillator to provide a low impedance on the bases when the transistors are turning "off".

Since a constant voltage is required on the oscillator to provide a constant frequency, a regulator which drops the supply to 10V is used. Due to the low power consumption of the oscillator, a dissipative regulator is used. By adjusting the output voltage of this regulator, the inverter frequency can be varied.

ROTARY TRANSFORMER - Three (3) transformer designs were made and fabricated throughout this program. The first and second ones were reported in the first reporting period. The first or so-called "Test Transformer" consisted of the largest cup core available at the time at Matrix, and was 7/8" in diameter and 5/8" long (Figure PD-1, Report #1). The winding space was wound full and tested for its capabilities with sine wave excitation (pages 4-6, Report #1). The results are summarized as follows:

Primary turns Secondary turns Output load 16 ohms Input volts 8.65 rms volts Input current 1.56 rms amp Output volts 7.42 rms volts Output amp 0.56 rms amp Frequency 10KHz Excitation current 1.48 rms amp Efficiency 98.7%

This is described in Appendix (I).

The second model was designed to have a rotatable secondary and was described in pages 6-26 of the first reporting period, with Figures PD-2, PD-4, PD-5, and PD-7. The construction was completed by the end of that reporting period. The detailed description of this model is found in Appendix (II).

The final (third) design accommodates the mounting of the transformer over a 1,000" outside diameter tubing which in turn supports
the solar panels. The connections from the panels thread the inside
of this tube, emerging at one end of the transformer to make connections to the primary terminals. At this point, part of the power
processing has been done already, since only alternating current
can pass through the transformer.

Nominally, 100 watts is required of this design. However, the transformer has negotiated about 320 watts for a short time with only moderate heating. With very little change in dimensions, this design can easily be made to handle powers of the 1000 watt level. Figure C shows the proportion and arrangement of the windings, core, and frame. The detailed calculations are given in Appendix (II), and construction details are shown in Figures 52 through 61.

PULSE WIDTH SWITCH - Figure 4A is a schematic of the first pulse width switch tested. This circuit has been successfully used in low power applications, however several problems made it undesirable for use at the higher power levels in this application. One problem is that the pulse width switch is DC driven and therefore the control circuitry ground is the same as the power ground. This causes considerable noise problems since there are high amperage ground currents in the power ground. A second problem is encountered due to the storage time of the switch transistor. When Q3 turns "on", it turns Q1 and Q2 "off", bringing point A to ground. Since E1 + E2 is only 3V to 4V, little power is lost in R3. However, during the period that its storage time keeps Q1 turned "on", E2 + E3 + E1 appears across R3, which can amount to a significant power loss. A third problem is the necessity of returning R3 to a negative bias in order to rapidly and completely turn "off" Q1 and Q2.

6.3

はなるというないというないという

In order to overcome some of these problems, the pulse width switch was changed to the circuit of Figure 4B. Here the drive to the switching transistor is AC coupled by transformer Tl. With this circuit, it is not possible to obtain a 100% duty cycle on the switch, however this is not a significant problem since for the loop to operate properly, a 100% duty cycle must be avoided. With the drive AC coupled, the controller ground can be kept separate from the power ground. Transistor Q5 is used to drive the transformer, and Q5 is in turn switched by Q6. Tl-A is used to provide some regeneration to Q5 in order to improve the switching speed.

With this circuit, the storage time of Q4 causes no severe problems. The switch simply stays on for the length of the pulse width signal plus the storage time of the transistor. In this way, there is no power loss associated with the storage time.

As with the inverter, the best efficiency is obtained in the series switch if its base drive is proportional to its collector current. This is accomplished by inserting two windings of a current transformer in series with the inverter outputs before they are rectified. The secondary of this transformer is full wave rectified and filtered and used as the supply voltage for T1. This supplies a certain number of amp seconds to be used to drive the base of the series switch. Since the number of amp seconds out of the inverter is the same as the amp seconds through the series, switch, the base drive of the series switch is proportional to its collector current.

PULSE WIDTH CONTROL - The pulse width control circuitry has also undergone changes from that shown in the second quarterly report (Figure 5). This circuit utilized a differential amplifier to compare the DC input signal against a ramp generated by a current source feeding a capacitor, the capacitor being discharged each half cycle of the inverter by transistor Q7. The jitter is introduced by varying the current source output.

The problems encountered with this circuit are:

- 1. If the input signal became too high, then the output signal goes to a 100% duty cycle and the jitter is lost. This is not permissible for proper operation of the maximum power controller.
- 2. The rise and fall times of the pulse width signal were not sufficiently fast.
- 3. Since the differential amplifier must compare voltages close to ground, a negative bias supply is required.
- 4. The square wave signal from the secondary of the RPT has transients which require that the waveform be reshaped before it is used to synchronize the pulse width controller.

The redesigned circuit is given in Figure 19. Instead of using a fixed current and a variable comparator, this circuit uses a variable current source with a fixed voltage comparator (Schmitt trigger). Capacitor C23 is as before discharged by Q25 at each half cycle of the inverter waveform, however the output of the RPT is shaped by transistors Q33 and Q34 before it is used to trigger Q25. R41 plus R44 set a maximum time in which capacitor C23 will be charged to the firing level of the Schmitt trigger, and therefore set a maximum duty cycle that can be obtained. The jitter is introduced by shunting R44 with Q26, and therefore varying this maximum duty cycle. This circuit therefore sets a maximum duty cycle and insures that the jitter will not be eliminated.

The Schmitt trigger provides the required fast switching waveform to efficiently drive the pulse width switch.

東京大学を変えてきる。 ままいたません かんかん あんちゅう

POWER RECTIFIER - The output of the rotary power transformer is rectified by a pair of diodes and filtered by a single capacitor. After being rectified and filtered, the output of the rotary transformer is then again chopped by the pulse width switch of the main switching regulator.

The second secon

The possibility of combining the functions of rectification and pulse width switching into one operation can be seen to hold possible advantages, insofar as greater efficiency is achievable through the removal of one voltage drop and greater reliability through the reduction in the number of components. After study, however, one finds that in this application the only semiconductor devices that are designed for this sort of application are SCR's.

The semiconductor device required must be capable of handling a minimum forward current of 5 amps and be capable of blocking at least 50V in the reverse direction. A preferred device would be capable of handling a minimum of 5 amps in the forward direction and be capable of blocking 50V in the forward direction and 100V in the reverse direction. The lesser requirements are produced by a circuit which uses two chokes and two recirculating diodes requiring that the switching device block only in the reverse direction. This system, however, requires the use of much larger chokes, since the choke must supply energy for greater than one-half cycle, and more current flows through the recirculating diodes, which results in higher losses.

The design of transistors is such that they do not readily lend themselves to this type of function, being designed to conduct and block in the same direction. In the reverse direction, a transistor must block with the base-to-emitter diode which normally has a 5V to 15V breakdown rating. If the circuit utilizing two chokes and recirculating diodes is used, there is no necessity of blocking in the forward direction, so that if the transistor is used in the inverted mode (swapping emitter and collector functions), the reverse blocking can be accomplished. The problem with this configuration is that the beta in the inverted mode is less than one at high currents (greater than 1 amp). The drive required, therefore, makes transistors used in this configuration more lossy than diodes.

One device that will meet the breakdown and conduction requirements is a silicon controlled rectifier. The disadvantages of this device are:

- 1. It has a high forward drop, since it has a diode in the forward path;
- 2. It is considerably slower than a fast switching transistor; and

THE PARTY OF THE P

3. It requires a more complex driving circuit.

A circuit using SCR's as synchronous rectifiers was breadboarded and tested. The circuit is given in Figure 6. The output of the RPT was fed to two SCR's and the output of the SCR's was filtered by L3 and C3, with CRl being the recycle diode which allows the choke to supply energy to the load during the SCR "off" time. The SCR's were switched "on" by a blocking oscillator (Q1, T2) and turned "off" by the negative-going input waveform. Commutation between the two SCR's was automatically accomplished by the AV square wave input to the SCR's.

The circuit worked well with the exception that the efficiency was poor (Approximately equal to 75% at 100 watts). There were several causes of this low efficiency.

First, as mentioned above, the switching time of an SCR is slow. (The SCR's used were Transitron 2N1773A's with a rise time of lus and a fall time of 5µs. This SCR type is one of the fastest available) Since during the switching time there is both current through the device and an in-phase voltage across it, power is dissipated.

Secondly, on turn-off the voltage across the SCR is reversed and due to the slow fall time, large reverse current transients are produced which further reduce efficiency. Ll and L2 were added to reduce these reverse currents. Considerable reduction was accomplished, however, the required chokes were large enough to interfere with the forward operation. Diodes in series with the SCR's will solve this reverse current problem, however this eliminates one of the main reasons for synchronous rectification, namely to reduce the number of series semiconductor drops.

The third problem with the synchronous rectification and probably the most significant is the effect it has on the operation of the inverter. If the inverter is full wave rectified and filtered, the inverter is continuously loaded and the output current to a first order

is constant (with a short discontinuity during switching). With the synchronous rectification, however, the loading is not continuous, the inverter being loaded only during the "on" time of the synchronous rectifiers. If the same amount of power is to be handled by an inverter feeding a synchronous rectifier system as one feeding a full wave rectifier and filter, then the inverter feeding the synchronous rectifier must have a current which is one divided by the duty cycle times the current of the inverter feeding a full wave rectifier. Since the circuit being designed must operate over a wide input voltage range (16.6V to 50V), the duty cycle at the maximum operating voltage is low (approximately equal to 25% or . 25). The inverter feeding the synchronous rectifiers must therefore handle four times the current of the inverter feeding the full wave rectifier and filter. This causes considerably more I2R losses both in the transformer windings and in the transistors, and therefore reduces the efficiency.

Also, during switching of the inverter transistors, the inverter is unloaded (the switching of the inverter having turned off the SCR's) creating higher transient switching voltages in the inverter.

THE PROPERTY OF THE PARTY OF TH

The conclusion, therefore, was to use a full wave rectifier and filter the output of the inverter, and to follow this with a transistor pulse width modulated switch.

MAXIMUM POWER CONTROLLER - During the course of this program, two different techniques of achieving maximum power were investigated. The first technique was to measure the power at some point in the path from the solar cells to the battery and maximize this power. The second technique was to maximize the current out of the unit and thereby achieve maximum power.

The two approaches require the same types of circuitry with the exception that the power measuring technique requires a power measuring circuit while the output current maximizing technique requires that the output current be sampled.

Figure 7 is a block diagram of either system, depending on whether the circled block is considered a power measuring circuit or a current measuring circuit. (It should be noted, however, that although the power measurement circuit is shown at the output, it could be placed anywhere in the forward path as discussed in Appendix (IV). The current sample circuit, however, must be at the output).

6.6.1

POWER SENSOR TECHNIQUE - The first system to be bread-boarded and tested was the maximum power sensing circuit. The power sensor was a multiplier circuit which multiplied the current flowing through the rectifiers times the voltage on the output of the rectifiers. The current was sampled by means of a current transformer in series with the rectifiers (Figures 8 and 9, Table I). The output of the current transformer is full wave rectified, filtered and fed into a resistive load. The voltage across the resistor is now proportional to the current through the rectifiers.

The current sample is then fed into the multiplier along with the voltage at the output of the rectifiers. For the specific use intended here, the absolute value of the power being measured is of little significance, and the desired output is actually the variation of this power level as the effective load is jittered by some small increment. This allows scale factors to be chosen for convenience, and tends to minimize the effects of non-linearities occuring outside the range of interest.

The multiplier consists basically of a duty cycle modulator, a switch, and an averaging filter. Multiplication occurs in the following fashion: If a voltage is applied to the input of the switch and the duty cycle. or ratio of "on" and "off" times of the switch is varied, it can be seen by inspection or shown by a Fourier analysis of the resultant waveform that the average output of the switch is the input voltage times the duty cycle. Consequently, if this average output is then detected by means of an averaging filter, the output of the filter will be a product of the input voltage and the duty cycle. If in turn the duty cycle is made proportional to some other parameter, in this case specifically the bus line current, the result is the product of the bus line current and voltage, which is, of course, power. This assumes only that the rates of variations in the two parameters being multiplied are sufficiently slower than the switching rate of the duty cycle modulator so that the output can be properly filtered without attenuating the variations caused by either input.

Detailed operation of the circuit (Figure 10) is as follows: Transistors Q2 and Q3 form a differential pair which functions as a voltage comparator. The emitters of Q2 and Q3 are fed by a constant current source comprised of transistor Q4 and associated resistors.

The purpose of the constant current source is to hold the operating point of the differential stage constant with relatively wide swings at the two inputs, and to provide maximum coupling between the two halves of the differential amplifier. The base of Q2 is driven with a linear ramp generated by constant current generator Q1 and associated resistors, which charges capacitor C1 at a linear rate. The ramp is reset to ground once per cycle of the main oscillator by shunt switch Q8 which is driven by a differentiated output from the oscillator. The output of the current sample circuit is fed to the other input of the voltage comparator which is the base of Q3.

If the action of the circuit is considered from the time the ramp has been reset, it may be seen that Q3 at this time is conducting, which in turn causes Q7 also to be in the "on" or conducting state through the action of the driver transistors Q5 and Q6. Excessive gain is used between the output of the comparator and the switch transistor Q7 in order to sharpen the switching time. As the ramp rises, it ultimately reaches an amplitude where it equals or slightly exceeds the voltage at the base of Q3 and causes the differential amplifier to swing in the opposite direction, i.e., Q2 conducting and Q3 heading toward cut-off.

When this condition occurs, Q7 will go to the "off" state, again through the action of driver transistors Q5 and Q6. When Q7 is in the "off" state, the clamping diodes, CR1 and CR2, in conjunction with the current source Q8, hold the output of Q7 at ground level. If the ramp is linear, the time required to reach this state is a function of the voltage at the base of Q3, which is in turn a function of the current through the main bus. As this level is raised and lowered, the duty cycle of the series switch Q7 is raised and lowered in direct proportion to the control signal. The output of Q7 is averaged by means of a multisection RC filter in order to obtain the average value which then yields the desired product term.

Test results on the multiplier are tabulated in Table 2, and plotted in Figure 11. E_8 was held constant while E_1 was varied through its operating range. This was then repeated for various levels of E_8 . For a given E_8 value, the output of the multiplier should be a linear function of E_1 . This is demonstrated in Figure 8. It can be seen, however, that there appears to be a small offset in the output. This is caused by miss-match in the differential amplifier, storage time in the series switch, transistor Q7, and the finite rise and fall times of the output of Q7. In operation, however, the multiplier is never required to operate at less than a 20% duty cycle, so that the non-linearity at low levels causes no problems.

An obvious alternative approach to the duty-cycle modulation portion of both the multiplier and the main power controller would be the use of a magnetic amplifier as the current or voltage-to-duty cycle converters. A cursory examination of the alternatives indicate that although the magnetic amplifier has certain advantages, specifically in that its control winding may be placed directly in a DC line thus providing a convenient point to sample the direct current. It does suffer from certain disadvantages which tend to reduce the desirability of this approach. The magnetic amplifier is basically a non-linear device requiring the use of fairly extensive feedback to guarantee the multiplier output being a reasonably linear function of the true output power.

Additional circuitry is necessary to obtain reasonably fast switching waveforms from the device without dissipating excessive power. This approach is relatively inflexible in that any type of scale change must be effected by redesigning and rewinding the device. It is somewhat expensive to build in the special configurations required for this application. It also has a rather slow response speed if one attempts to derive much gain from it. While not particularly important for this specific usage, it would tend to narrow the range of possible applications for the multiplier device.

The output of the multiplier is coupled into an AC amplifier which amplifies the jitter frequency signal to approximately 8V peak-to-peak. This signal is then fed into a synchronous detector (Figure 12). The function of this detector is to provide a DC output as a function of both the phase and amplitude of the jitter frequency output of the multiplier. To accomplish this, the jitter frequency output of the multiplier is AC amplified and synchronously detected by means of a shunt chopper which is driven by the jitter generator. This drive signal is phase shifted somewhat to compensate for the phase shift in the input signal to the detector which results from the response of the main pulse width regulator and the filtering of the main bus line.

Following the chopper is a 2-stage DC amplifier which boosts the signal level and in addition performs the final rectification. Although both a positive and negative output would be available from this circuit, the positive output only is taken since the single sided output is sufficient to control the main pulse width converter. The

「一般のできる」とは、これをいることが、これのはなっているできるとのできるという

control circuit operation is such that the output of the synchronous detector is essentially zero up to the point of maximum power, and then rises in a positively-going direction very sharply as the maximum power point is reached. This rise is commensurate with the phase reversal which occurs at the multiplier output at the point where maximum power is reached. The output is then fed to the main pulse width converter and used to control the duty cycle of the main regulator in such a manner as to hold the power drawn from the main bus at a point very near the maximum power level.

Problems of varying loop delays, however, created problems with the synchronous detector of Figure 12. It was therefore decided that better results could be obtained if the synchronous detector averaged the output of the amplifier during its sample time. This requires that the switch used in the synchronous detector be bilateral.

The revised synchronous detector circuit (Figure 20) uses a field-effect transistor (FET) to accomplish this objective. The output of the FET is filtered by C31 and C24, and then amplified by Q32 and Q33. This amplified signal is then fed into the pulse width control circuitry.

As described above, the circuit detects the phase reversal which accompanies the maximum power point. By averaging the amplifier over the synchronous detector sample period, much greater phase shifts in the jitter signal can be tolerated.

The jitter generator (Figure 21) consists of a 100Hz unijunction oscillator which drives a complementary flip-flop. The flip-flop therefore runs at 50Hz and provides the jitter signal to the pulse width controller and the synchronous detector.

Measurements taken on the maximum power controller described above are given in Tables 3 and 4. Figure 13 is a block diagram of the test setup. In Table 3, the two column headings are "controller maximum" and "manual maximum". In the "manual maximum" testing, the control input to the pulse width controller was replaced by a variable voltage source allowing the pulse width to be manually controlled. This control was then adjusted to give the maximum output power and the various voltages were recorded under "manual maximum".

Then the control loop was closed and the circuit was allowed to find its maximum. The resulting parameter values are listed under "controller maximum".

Ideally, the two columns should be identical. However, since the power measuring device is not located at the output of the circuit, it attempts to maximize the power into the pulse width switch and the resistor. Since the pulse width switch has a series resistance, there is a difference between the maximum power out of the rectifiers and maximum power into the load. This discrepancy, however, is less than 2%, and in practice would not be a problem.

Table 4 gives the variation of input and output power due to load changes. As the load is changed by a factor of 6, the inverter input resistance R_{in} changes less than 2%, indicating close tracking of the maximum power point. R_{in} is approximately 21.5 Ω . For maximum power transfer from the source, R_{in} should be 20 Ω , however. The power sensor is located at the output of the inverter, and therefore tries to maximize the output power from the sourceinverter combination. This tends to increase the value of R_{in} .

6.6.2

CURRENT SENSOR TECHNIQUE - The second approach to maximizing the available power is to maximize the current into the load. The circuitry necessary to accomplish this requires only that the power measuring circuit be replaced by a circuit that samples the output current. As with the power sensor, only the variations in the output current caused by the jitter frequency are necessary; the output current sample therefore need consist only of a current transformer. The output of the current transformer is filtered (to remove the ripple at the inverter frequency) and fed into the amplifier (Figure 22).

During discussions with Mr. Leo Veillette (the NASA technical representative on the contract), it was decided that the output current maximizing technique would be the best choice to pursue. This conclusion was reached for several reasons: First, the output current sensor requires only a transformer while the power sensing circuitry is quite complex and must be accurate for good operation. Second, the output current sensing technique is both lighter and more reliable, and third, although the power sensing technique is more general than the output current sensing technique, in this application the output current sensor provides better results. This is due to the fact that the output current sensor matches the load to the entire power conversion system, thereby providing maximum power into the load. The power sensor, however, matches the pulse width converter to the solar array and inverter, and thereby provides maximum power to the pulse width converter and load, combination which is not maximum power to the load.

The power sensing technique could provide maximum power to the load if the power sensor were placed at the output. This, however, would require the use of additional circuitry in order to accurately sample the output direct current.

TRICKLE CHARGE CONTROLLER - Although it is required in the contract that the design only be capable of constant current controlling (the circuitry not being supplied), it was felt advantageous by Matrix and the NASA technical representative that the circuitry be included on the breadboard.

The constant voltage mode in which the design must also be capable of operating is not included on the breadboard. Since the techniques for accomplishing this are quite standard, little would be gained by including this capability on the breadboard. This mode of operation is demonstrated in the spacecraft electronics converter which is part of the spacecraft power simulator, where a pulse width regulator similar to the one in the maximum power controller is used to produce a constant voltage output.

The breadboard can therefore operate in two modes -- maximum power, or constant current (trickle charge). This is accomplished by the use of two control loops which are selected by the battery third electrode sensor. When the battery is in a discharged state, the third electrode sensor activates the maximum power loop. When the battery reaches approximately 80% of full charge, the third electrode sensor is tripped which causes the breadboard to shift to the constant current mode.

<u>SPACECRAFT POWER SIMULATOR</u> - In order to properly test the operation of the breadboarded maximum power controller, it was necessary to provide inputs and outputs similar to those which would be seen on a spacecraft.

For this purpose, a simulated solar array, simulated battery, and a typical spacecraft electronics load were designed. These units were built into a rack and panel in order to provide a convenient test setup. Figure 14 is a sketch of the front panel of the spacecraft power simulator. Input and output connections are made by means of color coded binding posts. Since considerable power is dissipated in the simulator, a muffin fan was incorporated to provide cooling. When the power simulator is in use, the fan should be turned on; otherwise, damage to the power simulator will result.

SYSTEM TESTING - Due to time limitations, only enough testing was done on the final breadboard of the maximum power controller to ensure that the system met specifications. This was due in part to the time spent in designing and construction the spacecraft power simulator. The time spent on the spacecraft power simulator was considered a good investment since it considerably simplified testing and also provided realistic test conditions. Furthermore, considerable testing was anticipated at GSFC upon receipt of the breadboard.

Table 5 contains the final test data taken on the breadboard prior to shipment. Figure 15 is a diagram of the test setup. All the output power of the maximum power controller is fed into the battery simulator to simplify measurements. The input and output currents and voltages were measured, and the input power, output power and efficiency were calculated. The system efficiency exceeds the required 83% over the specified temperature range.

THE REPORT OF THE PARTY OF THE

The trickle-charge current was also measured and recorded at the temperature extremes. Due to temperature variations in the magnetic core of the trickle-charge sensing transformer, there is a possitive slope of current versus temperature. A simple resistor thermistor temperature compensating network can be used to flatten the shape, if desired. The trickle-charge level can be adjusted by R112.

TECHNICAL SECTION - Figure 16 is a schematic of the maximum power controller breadboards supplied to NASA by Matrix. The maximum power controller is divided into two breadboards; the smaller section being the inverter and the rotary power transformer; the larger breadboard contains the rectifiers, switching regulator, and the control circuitry.

Figure 16 is divided into several sections by the dotted lines. Each of these sections is a functional block. In the following text, the overall operation of the circuit will be discussed, followed by a description of the function of each section of the circuitry.

The purpose of the overall system is to take the power generated by the solar cells, transfer this power from the rotatable solar panel to the spacecraft, and then transform it to levels usable by the spacecraft battery and electronics. Also, the system is designed so that it maximizes the power available to the spacecraft and battery. Should more power be available than can be used in the spacecraft (battery fully charged), the system has provisions for shifting to a secondary mode in which it trickle-charges the battery while supplying power to the spacecraft electronics. The system is designed to operate in conjunction with sealed nickel cadmium batteries which have a third electrode for sensing the charge state of the battery. The signal on this third electrode determines the mode in which the system is to operate (maximum power or trickle-charge).

The power from the solar array is chopped by the inverter. This voltage is then coupled through the rotary transformer. The secondary of the rotary transformer is full wave rectified, filtered, and then fed to the pulse-width switch. The pulse-width switch reduces the rectified voltage to the proper level to supply the battery and the spacecraft electronics. The pulse-width switch is controlled by either of two control loops, depending on whether the operational mode is maximum power or trickle charge.

In the maximum power mode, the operation of the circuit is as follows: The jitter generator introduces a 50Hz square wave component on the 20KHz pulse width signal. This causes a 50Hz variation of the output current (since the load is a battery, the output voltage is forced to remain approximately constant so that a pulse width variation shows up as a variation in the output current).

This 50Hz component of the output current is sensed by the current transformer primary on the output. The current transformer secondary is filtered to remove the 20KHz pulse width modulation frequency and the 50Hz output of the filter as then fed to the synchronous detector. The synchronous detector averages the amplifier ourput during its sample period (which is every other half cycle of the jitter generator). The output of the synchronous detector is positive when the output Δ_i is in phase with the jitter signal. The pulse width controller is designed such that a zero input signal from the synchronous detector produces a maximum pulse width, which is approximately 85%. The pulse width is purposely prevented from reaching 100% in order that the jitter signal not be lost. When power is applied to the system, it therefore starts operation at maximum pulse width. If the input levels and the load are within the control range of the system, the output Δ_i caused by the jitter generator will be in phase with the jitter signal. This will cause an output from the synchronous detector which will produce a positive control signal to the pulse width controller, thereby reducing the pulse width.

This process continues until the maximum power point is reached. At this point, the phase of the \$\Delta_i\$ output reverses, causing a loss of output signal from the synchronous detector. The system will therefore begin increasing its pulse width until the synchronous detector again produces a positive output voltage. The system will then remain at this point, which is at a slightly higher pulse width than the maximum power point. (The amount of difference between the maximum power point and the system operating point depends on the amount of loop gain. The maximum power controller has sufficient gain to make the difference between these two points negligible.)

The second control mode of the system (trickle charge) is initiated by the battery third electrode. In this mode, the battery current is regulated at a preset level. The spacecraft electronics load, however, is allowed to draw whatever power it requires. Operation is as follows:

The battery current is sensed by a single turn through the torroidal core of a magnetic oscillator. The current in this winding produces an unbalance in the core, and therefore asymmetry in the square wave output of the oscillator. The output of the magnetic oscillator is filtered, producing a DC level proportional to the amount of asymmetry in the oscillator and therefore proportional to the cur-

rent into the battery. This DC level is then compared to a zener reference by a differential amplifier. The output of the differential is then fed to the pulse-width controller which regulates the output current.

When the third electrode voltage is low, signalling the maximum power mode, the power to the magnetic oscillator is removed thereby disabling the trickle-charge control loop. On the other hand, when the third electrode voltage is high and the loop switches to the trickle-charge made, the jitter generator is disabled, preventing the operation of the maximum power control loop.

INVERTER - Figure 17 is a schematic of the inverter. It is basically a pair of transistor switches which alternately switch the ends of the primary winding of the RPT to ground. The center tap of the RPT primary is returned to the solar array output. Each switch collector therefore alternates between ground and twice the solar array output voltage, since the open circuit solar array output can reach 50V. The switches must be capable of withstanding at least 100V (transients caused by switching increase the required switch breakdown considerably above 100V). The switches should also have a low saturation voltage in order to operate efficiently. The transistors used are Solitron MHT7612's, which have a collector-to-base breakdown of 220V and a collector-to-emitter breakdown of 200V with a .6V collector-to-emitter saturation drop at 5 amps.

The bases of the switches are driven by a current transformer which is connected in series with the switch collectors. In this manner, the instantaneous collector-to-base current is a fixed ratio of 10-to-1 at any collector current. This drive circuit is both efficient, since it has no dissipative components other than the switches themselves, and reliable, since it contains few parts.

Since the drive circuit is not self-starting and since its frequency would drift with operating levels, a synchronizing oscillator was added to maintain a reasonably constant frequency and to start oscillations. This oscillator is a resistance-coupled saturating magnetic oscillator. In order to keep its frequency constant, it is supplied from a regulated voltage. This voltage is provided by a dissipative regulator which receives its power from the input voltage. Since the power required for the oscillator is low, a simple dissipative regulator was used instead of a more complex switching regulator. Changing the oscillator frequency can be accomplished by changing the zener diode which controls the oscillator supply voltage.

A winding on the current transformer is connected across the collectors of the oscillator. (A resistor is connected in series with the winding to limit drive currents) When the oscillator switches, its collector voltages oppose the voltage Vab created by the inverter. The oscillator voltage being higher than Vab (due to the inverter), current flows into the a-b winding in such a manner as to switch the inverter state. Once the switching has been initiated, the regeneration of the current transformer causes rapid switching. Transistors Qll and Ql2 were added from base-to-emitter

要は 華華 をきずいまとうかっと ない できっち

of the switching transistors in order to further increase switching speed and to reduce the storage time of the switching transistors. Q11 and Q12 are driven by windings from the magnetic oscillator.

Due to their high switching speed, transistors Q10 and Q13 are quite susceptible to damage from transients. Several diodes have been added to the inverter to provide protection for Q10 and Q13. CR3 and CR9 are 160V zener diodes and are tied from collector to emitter on the switches. Their purpose is to prevent transient voltages higher than the transistor maximum ratings.

Diodes CR4 and CR10 are used to prevent the collectors of the switches from going negative with respect to their emitters. Diodes CR5 through CR8 are connected in series pairs from base-to-emitter of the switch transistors. Their purpose is to prevent the base-to-emitter diode from reverse breakdown.

The inverter is required to operate at a 100 watt level (50V at 2.5 amps). The switch transistors are rated at 10 amps, however, making the inverter capable of considerably higher power operation. The inverter was successfully operated for a short time (5 minutes) at a 320 watt level (40V, 8A).

PULSE WIDTH SWITCH AND FILTER - Figure 18 is a schematic of the pulse width switch and its driving circuitry. The switch transistor itself is a Solitron MHT7612 (Q20), chosen for its low saturation voltage and high speed. Base drive is supplied to Q20 through transformer T4. The primary of T4 is driven by Q19, which in turn is controlled by Q18. Winding 5 and 6 on T4 provides regeneration, thereby increasing its switching speed. Since the positive and negative volt-seconds must be equal for T4, the duty cycle of Q20 must be less than 100%. In operation, the maximum duty cycle is approximately 85%. This is attained by driving Q3 for about a 70% duty cycle with the remaining 15% being added by the storage time of Q20. No effort has been made to reduce the storage time to a minimum, since it contributes no losses - the only consequence of the storage time being to extend the duty cycle.

Diede CR23 is used to prevent collector breakdown of Q20, while diede CR24 prevents reverse voltage from collector to emitter.

CR25 and CR26 are used to prevent reverse overvoltages from base to emitter of Q20. The base is clamped in the reverse direction at about 7V. This allows a 7V backswing on T4 (which resets the transformer), but will not allow voltage high enough to break down the base to emitter junction of Q20.

The drive power for the Q20 is obtained from a current transformer in series with the power rectifiers (T3). The primary consists of two windings, one in series with each rectifier. The phasing on these two windings is reversed, providing a balanced drive for the transformer. The transformer secondary is center-tapped and is full wave rectified and filtered by CR18, CR19, and C12. The DC voltage developed across C12 is then used as a supply for T4.

By selecting the proper turns ratio for T3, the base current of Q20 is made to equal approximately 1/10 of its collector current for any operating level.

Following Q20 is the recycle diode CR27 which provides a current path for the choke L2 when the series switch Q20 is "off". Since this diode must operate at the same current level and switching speeds as the series switch, a low saturation, fast recovery diode was chosen.

L2, L3, and C14, C15 form a two-stage LC filter which reduces the pulse width modulated signal to a DV level. The inductance of L2 must be high enough so that it is capable of storing enough energy to supply the output current during the "off" time of the series switch.

7.3 PULSE WIDTH CONTROLLER - The pulse width controller performs two functions:

1. providing the pulse width modulated signal to the pulse width switch, and

2. introducing a jitter signal into the pulse width modulation.

Figure 19 is a schematic of the circuit. The pulse width modulation is accomplished by charging capacitor C23 to a fixed voltage (E_C) . C23 is charged by a current source consisting of Q27 and R45. The charging current is controlled by the input voltage (E_X) . Since the time required for C23 to charge to E_C is proportional to the charging current, and the charging current is proportional to the E_X , the time required to charge C23 is proportional to E_X .

At the start of each half-cycle of the inverter, C23 is discharged by Q25. Q33 and Q34 are used to reshape the square wave output of the rotary power transformer. Their collector waveforms are differentiated and used to drive Q25.

R41 and R44 provide a minimum charging path for C23. Their value is chosen such that they will charge C23 to E_C in less than one-half of the inverter cycle, thereby preventing a 100% duty cycle. The jitter is introduced by shorting out R44 with Q26 at the jitter frequency rate.

The jitter produced in this manner is approximately proportional to the duty cycle, since as the charging current through Q27 is increased (decreasing the duty cycle), R41 and R44 contribute a smaller percentage of the total charging current, and therefore shorting R44 creates a smaller effect on the duty cycle.

A Schmitt trigger (Q29 and Q30) is used to detect when C23 has reached $E_{\rm c}$ volts. The output of the Schmitt trigger is amplified by Q31 and used to drive the series switch.

RECTIFIER - In the final design, the output of the RPT is full wave rectified by a pair of Westinghouse 379E diodes. The diodes were selected for fast recovery, low forward drop, and 250V minimum breakdown rating. The diode output is filtered by a 10 of Difilm metallized capacitor. This capacitor was chosen for its low dissipation. Since the pulse width switch draws 4 amp pulses which must be supplied by the capacitor, it is important that the capacitor be a low-loss type for highest efficiency. If it becomes desirable to use a smaller capacitor, a high current tantalum capacitor can be substituted with a small loss in efficiency.

SYNCHRONOUS DETECTOR - The output of the amplifier feeds into the synchronous detector (Figure 20). Synchronous detection is accomplished with a field-effect transistor (FET). The jitter signal from the jitter generator is used to drive the gate of the FET. When the jitter signal is at a positive 10V, the FET conducts in either direction. The amplifier output signal is connected to the drain of the FET, and the source is connected to a filter consisting of C31, C24, R63, and R64. The polarity of the DC signal appearing on C31 is a function of the phase relationship between the output of the jitter generator and the output of the amplifier, and therefore a function of the phase relationship between the output of the jitter generator and the current jitter at the output of the pulse width filter. Since the phase of the output jitter abruptly changes, 180° at the maximum power point is passed. The jitter generator and the output current jitter are in theory either in phase or 180° out of phase. In practice. however, this is not exactly true since there are phase shifts in the circuit. The phase shift, however, is not large enough to seriously affect the circuit operation.

Considering that there are only the two above-mentioned phase relationships, the magnitude of the voltage across C31 is proportional to the amplifier output and therefore proportional to the output current jitter.

The magnitude of the output of the synchronous detector is therefore proportional to the magnitude of the output current jitter with the polarity being a function of the phase relationship between the output current jitter and the jitter generator.

Q32 and Q33 are used to amplify the output of the synchronous detector to the level required by the pulse width controller.

7.6

JITTER GENERATOR - The jitter generator (Figure 21) consists of a 50Hz unijunction oscillator (Q39) which drives a trigger flip-flop (Q40 and Q41). A unijunction oscillator was chosen since it maintains a reasonably constant frequency over the required temperature range.

Q38 is used to disable the oscillator when the system is operating in the trickle-charge mode. It clamps the timing capacitor (C40) of the oscillator to ground, thereby preventing oscillation. The drive signal for Q38 is provided by the battery charge detector.

CURRENT SAMPLE AMPLIFIER - Since the current jitter is greatly attenuated as the maximum power point is reached and the current transformer has a 115-to-1 stepdown, the signal at output of the transformer gets down to the several millivolt range. In order to obtain a usable signal level, it is necessary to amplify the signal. This is accomplished by a 3-stage amplifier (Figure 22).

Three common emitter stages with emitter degeneration are used to produce an amplifier with a gain of approximately 1000. Resistors R68 and R79 provide DC feedback which set the quiescent operating level of the amplifier. Capacitor C36 shunts out the feedback, allowing the gain to increase with increasing frequency, and capacitors C37, C38, and C39 roll off the amplifier gain at approximately 700Hz. The result is an amplifier with 3 db bandpass of approximately 40Hz to 700Hz. This allows the amplifier to amplify the jitter signal fundamental plus several harmonics, but not the 20KHz pulse width signal.

CURRENT TRANSFORMER - The current jitter on the output is detected with a current transformer. The purpose of the transformer is to separate the AC jitter signal from the output direct current and bring the jitter signal to ground potential. The transformer is wound on a torroidal powdered iron core. This material was chosen since it is capable of operating at high flux levels. A large number of secondary turns (3000) was required in order to support the 50Hz jitter signal. Since the maximum input turns was limited (26 turns) by the allowable DC bias on the core, a current stepdown of approximately 115-to-1 resulted.

The transformer is terminated in a two-stage RC filter in order to filter the 20KHz pulse width signal from the current jitter signal.

BATTERY CHARGE DETECTOR - The battery charge detector is a voltage level detector which provides a signal indicating that the battery has reached full charge (Figure 23). The circuit consists of two sections: a detector that is designed to be mounted with the battery pack, and an actuator which provides the control signals to the system.

The detector is a tunnel diode oscillator. It is designed to break into oscillation at approximately 65 mv. The inductance in the oscillator is actually a transformer which allows the signal to be brought down to ground level. The detector is designed such that it can be used on any cell in the battery pack. Also, as many as desired can be used. The only power required for the circuit is that which it obtains from the third electrode itself.

In operation, the third electrode of the battery is loaded with approximately a 60 load. With this load, the third electrode reaches 60 mv to 70 mv at about 80% to 85% of full charge. This is considered a good charge level to switch at, since if only a few cells contain detectors (which is the more usual case), there is an allowance for differences in charge capacity between cells.

In the detector, the 6Ω load consists of the parallel combination of the tunnel diode oscillator and a 6.8Ω resistor. C52 smooths the oscillator current, causing the oscillator to appear as a resistive load to the third electrode.

On the breadboard, a 2400 resistor is included in series with the detector. This is done only to facilitate testing, since it is difficult to adjust a laboratory power supply in the 60 mv to 70 mv range. It takes approximately 2.7V on the 2400 resistor to obtain 65 mv on the detector.

The actuator section of the battery charge detector consists of a rectifier and a regenerative amplifier. The outputs of all the detector transformers are rectified into C53, which is the input to the amplifier. The amplifier is a direct coupled 2-stage amplifier. R103 provides some positive feedback, increasing the switching speed and also providing some hysterisis which prevents the circuit from oscillating about the trip level.

On the breadboard, only one detector is required to trip in order to cause an operating mode change from maximum power to trickle charge. If desired, however, some sort of proportional control between the detectors could be implemented by changing the amplifier "trip" level. Some form of majority logic could also be used such that one more than half of the detectors would have to trip in order to cause a mode change.

7.10
TRICKLE CHARGE CONTROL - The trickle charge sensor (Figure 24) is a DC current sensor that is placed in series with the battery input.

The DC battery charging current creates an imbalance in the magnetic oscillator composed of Q43, Q44, and T6. The imbalance created by the battery charging current causes asymmetry in the normal square wave output of the oscillator, the amount of asymmetry being proportional to the magnitude of the charging current.

The output of the magnetic oscillator is used to switch Q51 giving a pulse width modulated waveform on Q51's collector. The pulse width waveform is then filtered by C55, C56, R119, and R120, giving a DC voltage proportional to the battery charging current. This DC voltage is compared to a zener reference by a differential amplifier Q50. The output of the differential amplifier is further amplified by Q48 and Q49 and then fed to the pulse width controller.

Q42 acts as a power switch providing power to the magnetic oscillator and the pulse width switch. Q42 is controlled by the battery charge detector, and is turned on when the system is operating in the trickle charge mode.

CONSTANT VOLTAGE CONTROL - There is no provision for constant voltage operation on the breadboard. This type of operation, was not breadboarded, since it is a reasonably standard technique and would add little to the value of this program. In order to make the breadboard operate in a constant voltage mode, it would be necessary only to add a differential amplifier. This amplifier would compare the output voltage to a zener reference. The output of the differential amplifier would be a third input to the pulse width controller. Proper control circuitry would, of course, have to be included that only allowed one mode to function at a time.

The spacecraft electronics converter included in the test panel is an example of constant voltage operation. Its pulse width controller and switch design is almost identical to that of the breadboard. The control loop, however, functions as described in the preceeding discussion, producing a constant voltage output.

8. SIMULATOR SECTION

SOLAR ARRAY SIMULATOR - Figure 25 is a typical set of solar cell characteristic curves. It can be seen that a solar cell looks somewhat like a constant voltage supply with a series current limiter. The model could be improved further by adding series resistance to account for the slope of A-B. The temperature and illumination intensity characteristics of the cell can be simulated by varying the supply voltage and the current limiter.

This appears only to require a power supply which has a current limiter and an external series resistor. The current limiter found in most commercial power supplies, however, has too slow a response time to be useable. The current limiter, therefore, had to be incorporated into the simulator.

Figure 26 is a schematic of the solar array simulator. An adjustable 50V 5 amp power supply is connected to the input. Q1, Q2, and Q3 make up the current limiter, the current through R2 and R3 being sampled by Q3, with Q3 then controlling the Darlington pair Q1 and Q2. R3 provides adjustment of the current limiting level, and R2 is used to prevent operation at too high a current level. R4 is an adjustable series resistor which can be set to provide the desired A-B slope on Figure 25. The output of R4 is fed into the inverter of the maximum power controller.

BATTERY SIMULATOR - One of the two loads on the maximum power controller is the spacecraft battery pack. In order to simulate this load, a shunt regulator was used (Figure 27). When the voltage into the simulated battery reaches the zener diode CR28, voltage transistors Q21 and Q22 are turned on, preventing the voltage from increasing. A 27Ω resistor is included in series with the zener diode to provide a small current voltage slope to simulate the internal battery resistance. The simulated battery voltage is approximately 24V.

One peculiarity is encountered in the spacecraft power simulator due to the fact that the battery simulator, unlike an actual battery, cannot deliver any current. It is possible, therefore, to have the output voltage of the maximum power controller drop below the battery voltage if the spacecraft electronic load is large enough (or the power available from the simulated solar array low enough). The entire output current of the maximum power controller will then flow into the spacecraft electronics load and the output voltage of the maximum power controller will drop below the battery voltage.

If the power available from the solar array is increased at this point, the output voltage of the maximum power controller will not increase. The reason for this is that the spacecraft power converter is a constant power load, and it therefore draws the largest input current at its lowest input operating voltage. Since the maximum power controller is designed to maximize its output current, the system gets "locked up" at the lowest operating voltage of the spacecraft electronics converter. This situation of course does not occur with an actual battery, since the output voltage of the maximum power controller cannot go lower than the battery voltage. If the maximum power controller cannot supply the entire power requirements to the spacecraft electronics converter, the remainder is supplied by the battery.

If the maximum power controller "locks up" as described above, normal operation can be restored by momentarily disconnecting the spacecraft electronics converter, allowing the output voltage of the maximum power controller to increase to the simulated battery voltage.

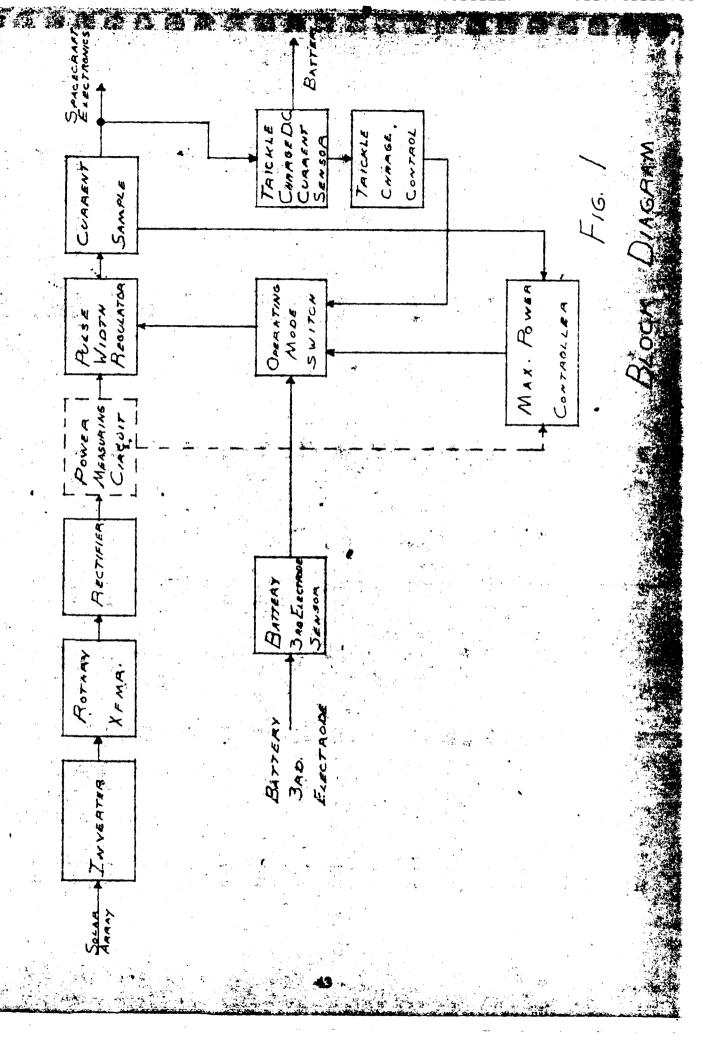
SPACECRAFT ELECTRONICS SIMULATOR - The second load on the maximum power controller is the spacecraft electronics. This load is simulated by a pulse width regulator with a resistive load (Figure 28).

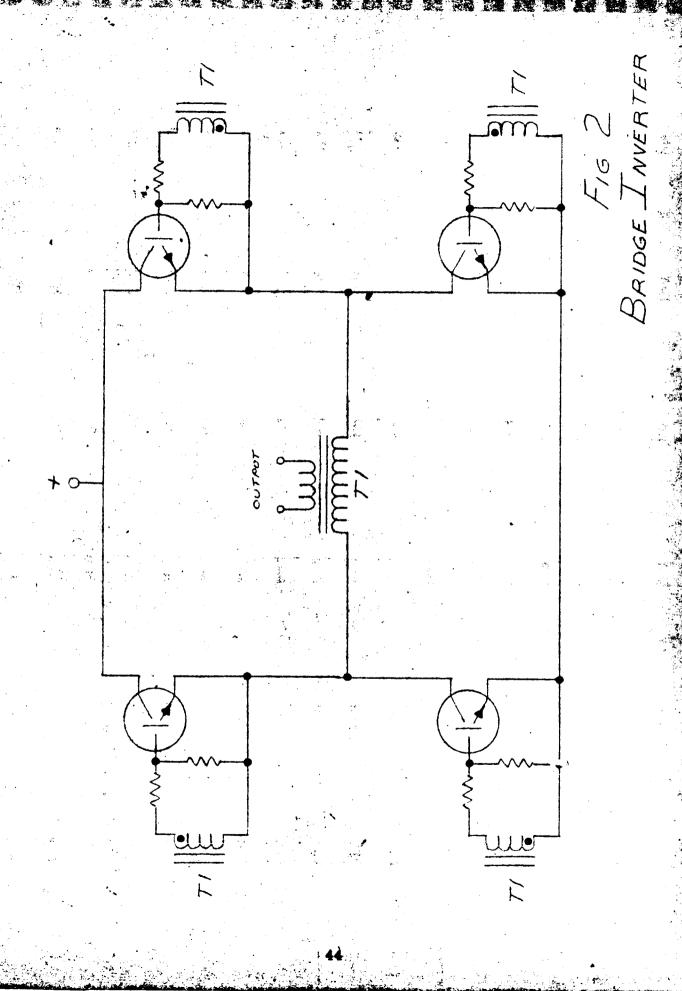
The pulse width control and switching in the spacecraft electronics simulator are almost identical to those circuits in the maximum power controller. The input to the pulse width controller, however, is the error signal from a differential amplifier which compares the output of the regulator to a zener diode reference. The output of the regulator is therefore a constant voltage (thereby indicating that the maximum power controller can be operated in a constant voltage mode).

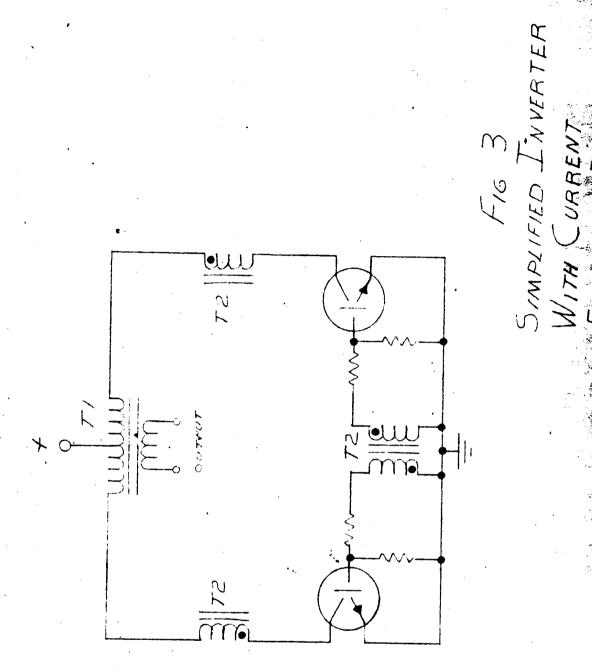
The 12V output of the spacecraft electronics converter can be patched on the test panel to an internal load which can be varied from 30 to 28Ω , or it can be connected to an external load.

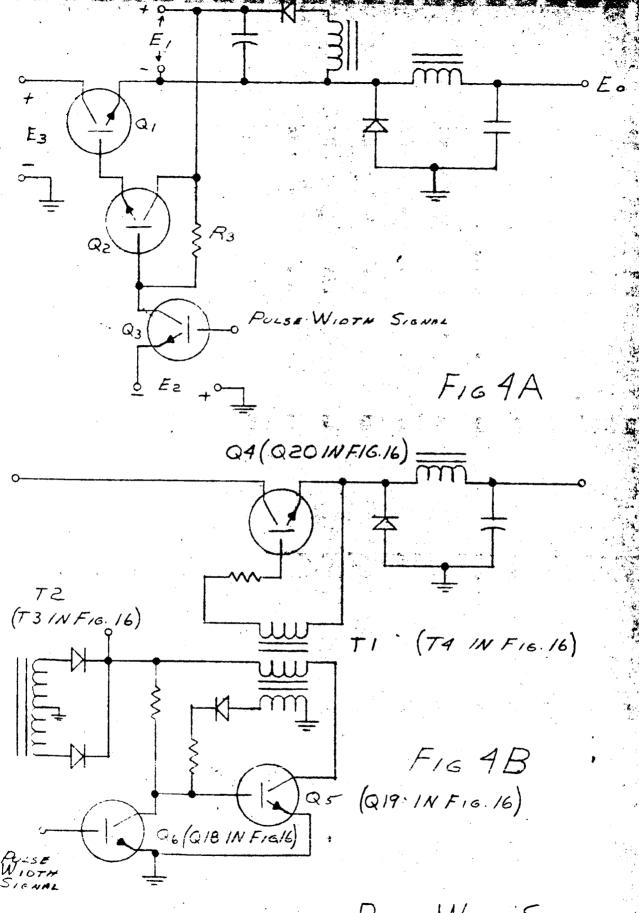
Three . 10 ± .25% resistors are included in the spacecraft power simulator to provide a means for accurately measuring the input and output currents. One of these resistors is located at the output of the solar array simulator, allowing the current into the inverter to be measured. The second resistor is on the input of the battery simulator, with the third being on the input of the spacecraft electronics simulator. By connecting an accurate digital voltmeter across the resistor binding posts, the currents can be measured to approximately .25%. Since the resistors are .10, the voltage-to-current conversion is 10 amps/volt.

When measuring the input and output voltages of the maximum power controller, care should be taken to measure the voltage on the side of the current measuring resistors towards the maximum power controller. Otherwise, the power dissipated in these resistors will be included in the maximum power controller losses, causing an error in efficiency measurements.









PULSE WIDTH SWITCHES

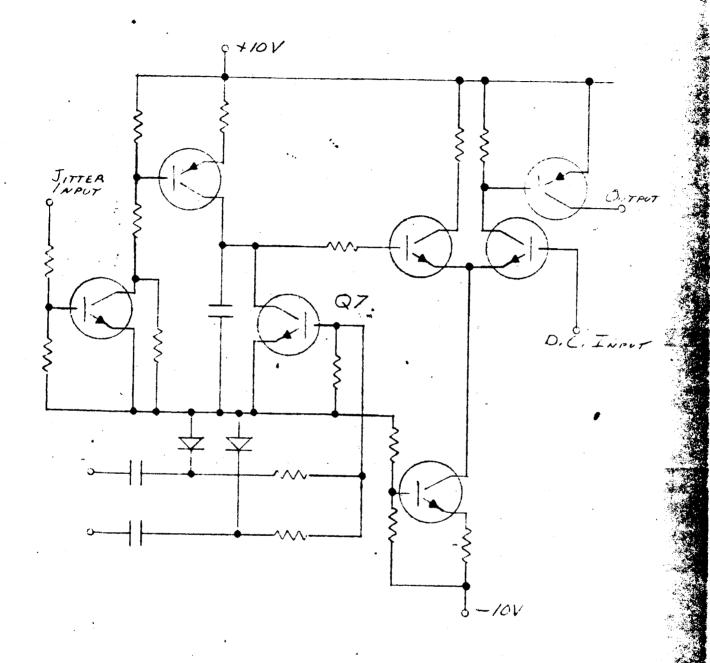
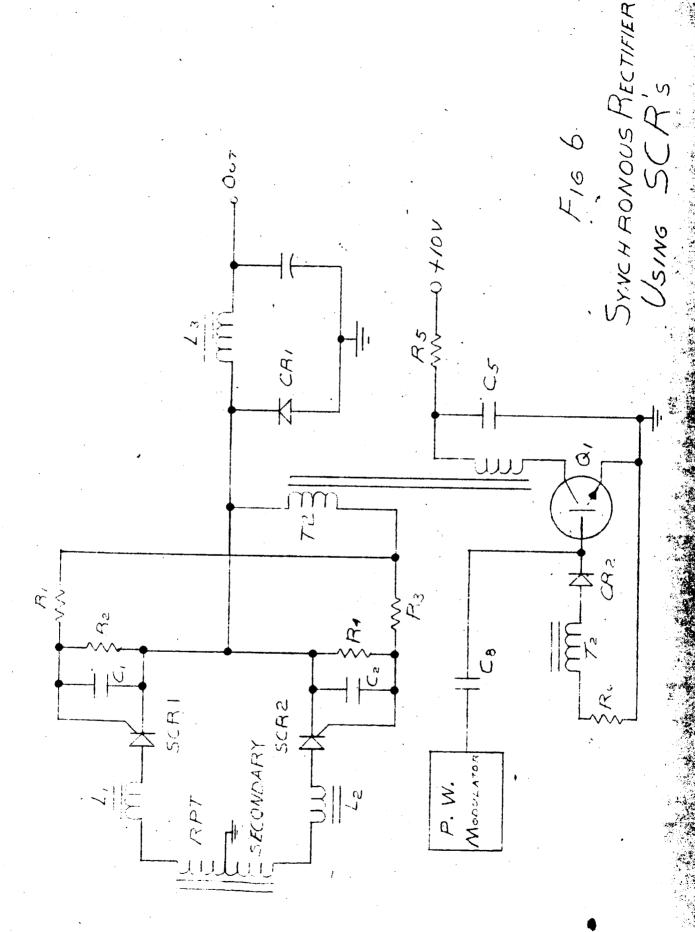
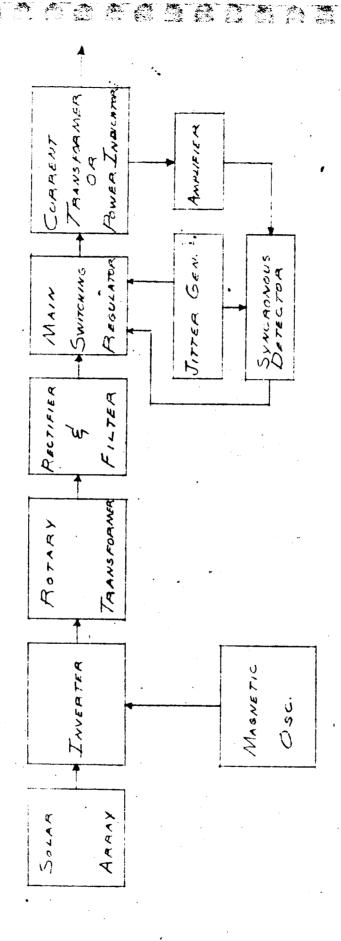
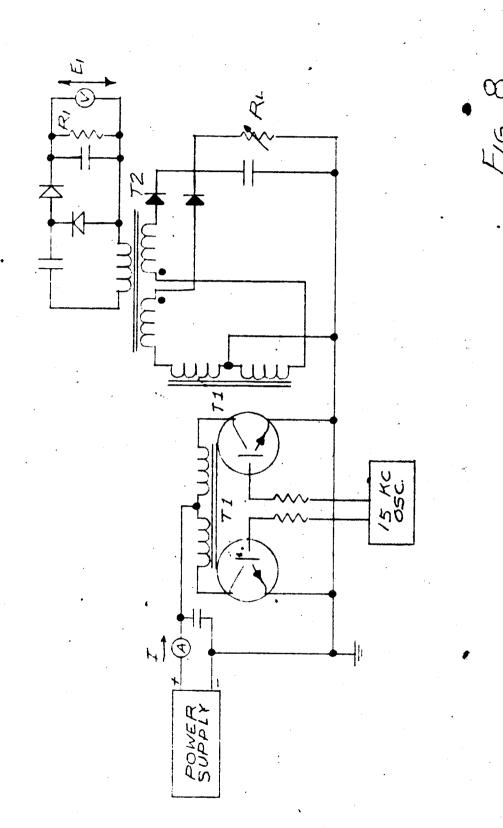


FIG 5 PRELIMINARY P.W. CONTROLLER

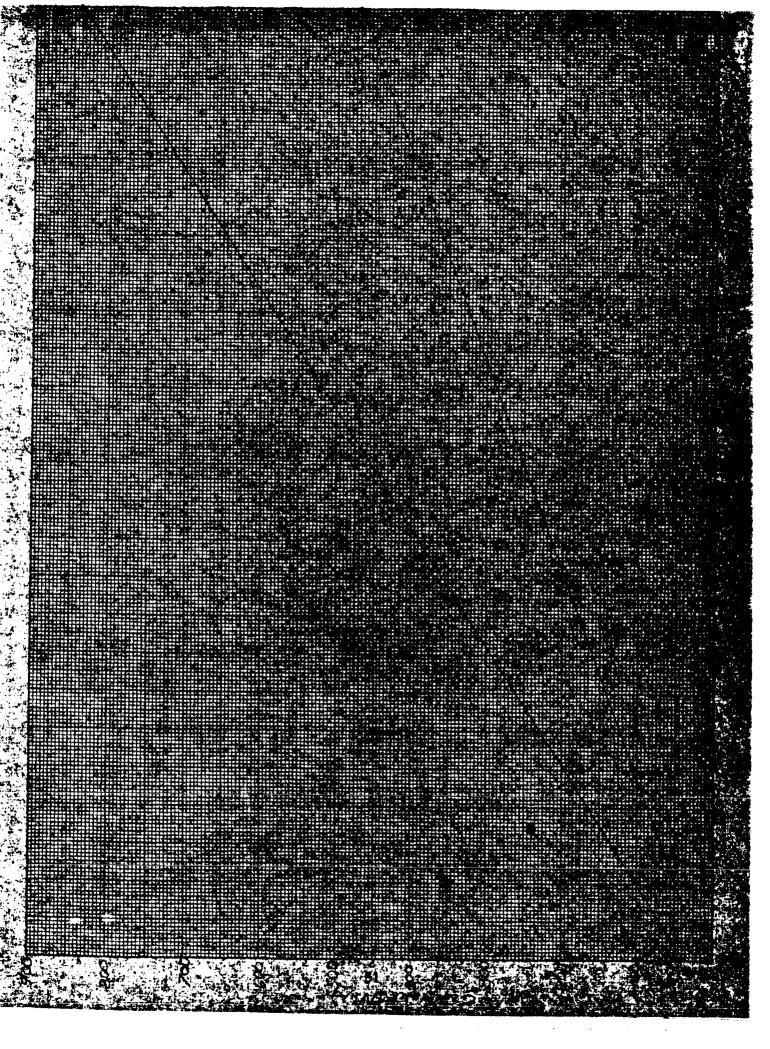


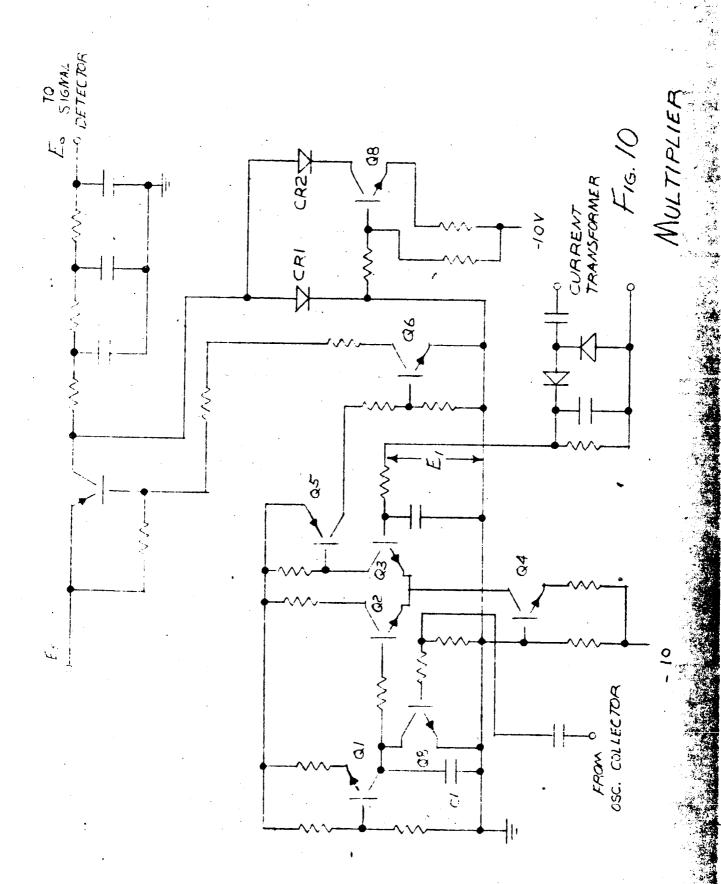


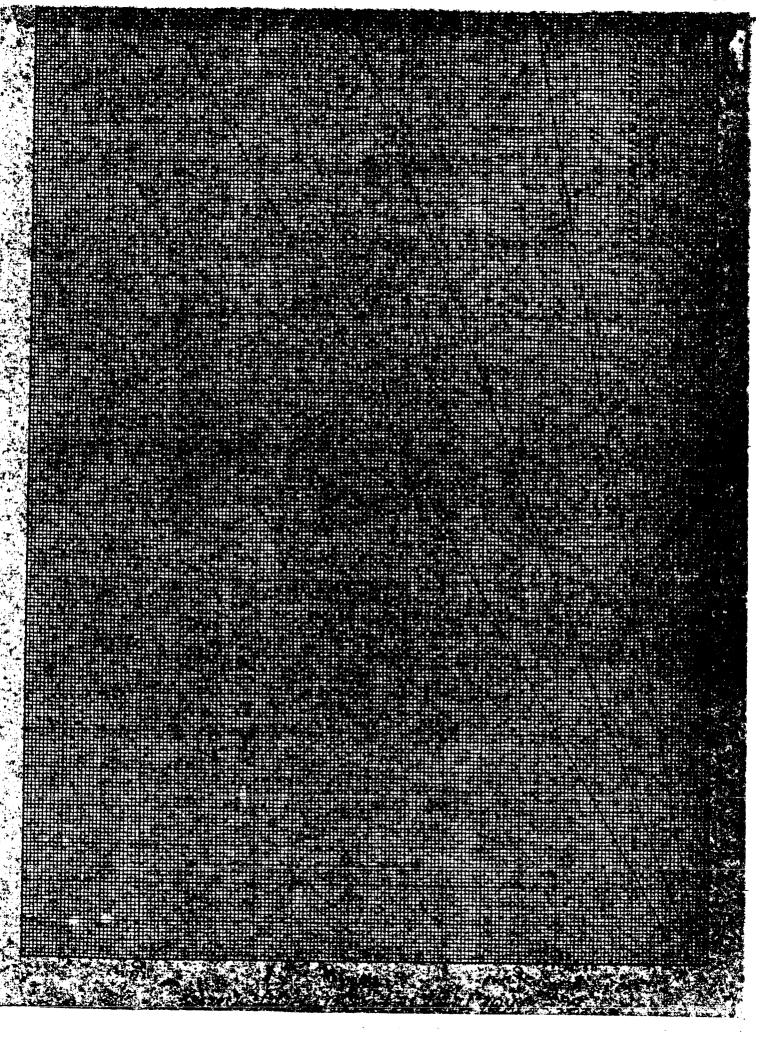
BLOCK DIAGRAM

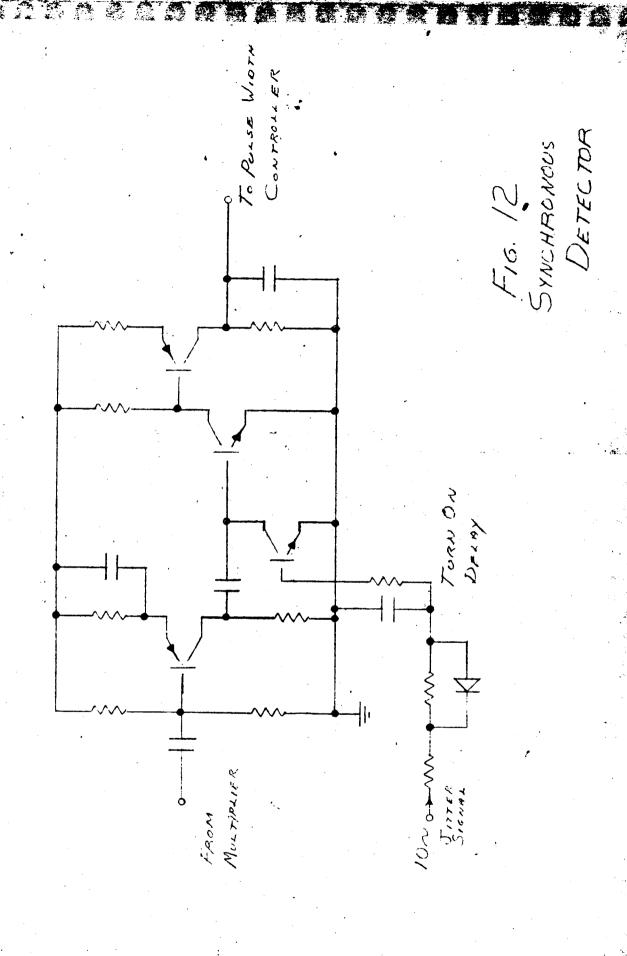


CURRENT SAMME CKT & TEST SET UP









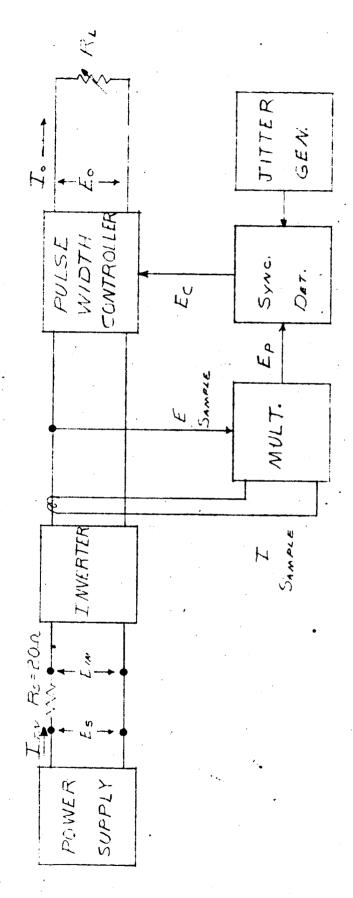


FIG 13 TEST SET UP FOR POWER MEASUREMENTS

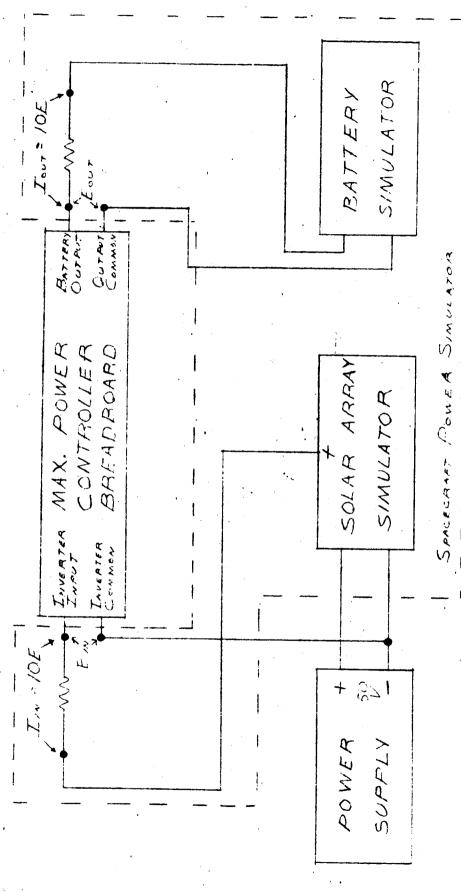
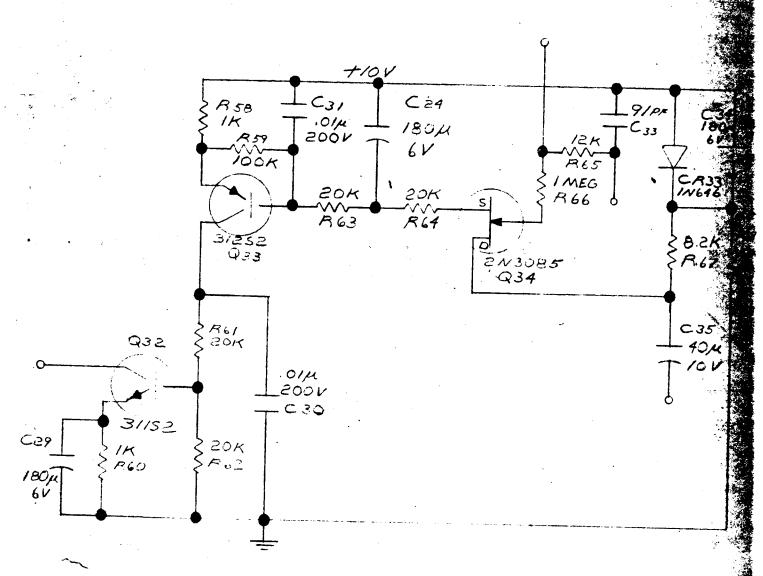


FIG 15 EFFICIENCY TEST SET-UP.

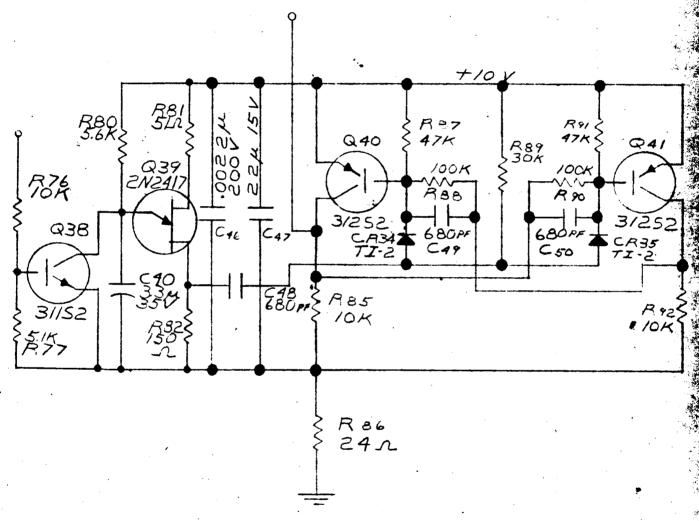
	/ 'Al	PLICAT	ION OF	REVISIONS				
	USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED	
[PD							
							1.4	
							1	



F16. 20

NLESS OTHERWISE NOTED MENSIONS ARE IN INCHES	DR. 7.5.7	DATE 3,66	
LERANCES	CHK.		Watix RESEARCH AND DEVELOPMENT CORP.
FRAC. ± 1/64 ANGLES ± 1/4	ENG. APPD		TITLE NABHUA, NEW HAMPSHIRE
SURA	MFG. APPD		SYNCHRONOUS DETECTOR
THE			- Opicini One Depet Por
			SCALE OWG. A 1201
			A-4304
	and the same that the same to be		Cope

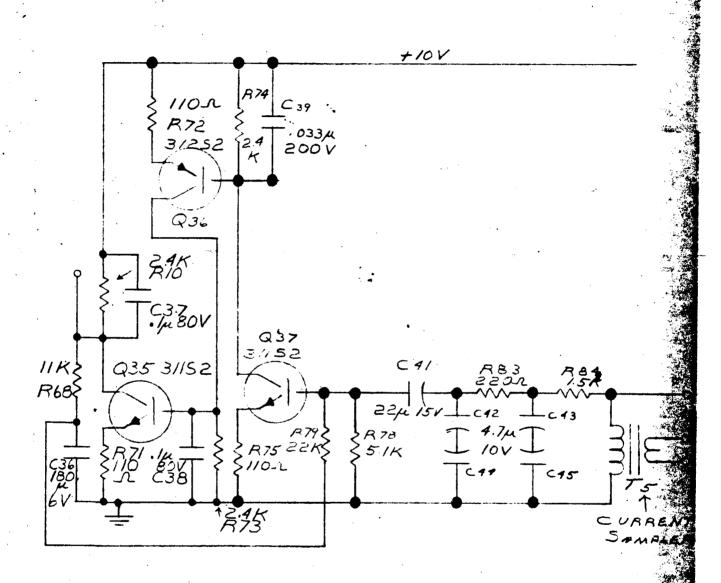
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVE
PD	4.					1
						19.5



. Fig. 21

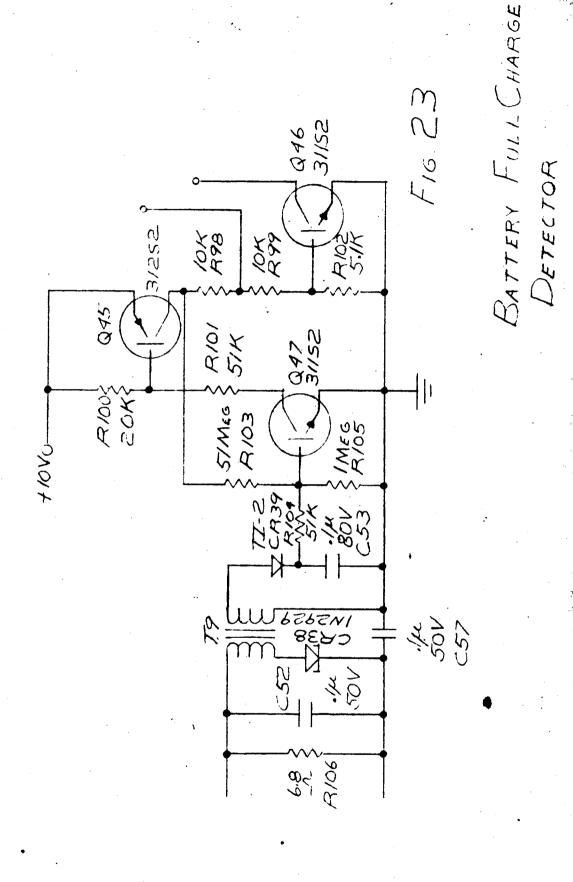
UNLESS OTHERWISE NOTED JIMENSIONS ARE IN INCHES OLERANCES DEC. ± .008 FRAC. ± 1/64 ANGLES ± 1/4	CHK. ENG. APPD	BATTY 8/66	Matrix Research and Development Corp. NASHUA, NEW HAMPSHIRE				
AAT'L:			J. ITTER	GENERATOR	***		
			9CALE	DWG. A- 4306			
		X	63	COOR	OF		

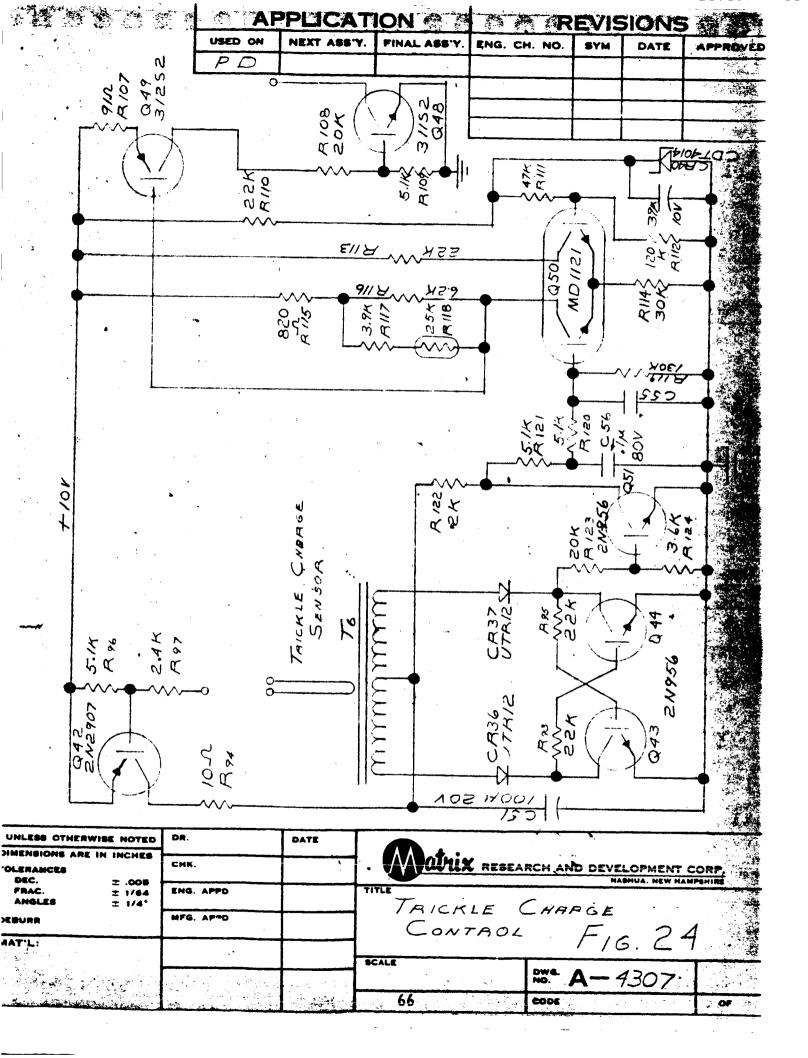
* A	PPLICAT	ION:	R	EVIS	SIONS	
USED ON	NEXT ASSY.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
PD						
· ·						



F16.22

MENSIONS ARE IN INCHES	DR.	DATE	A .		34	
LERANCES	СИК.		WOUX RESEAT	RESEARCH AND DEVELOPMENT CORP.		
FRAC. ± 1/64 ANGLES ± 1/4'	ENG. APPO		TITLE	SAMPLER		
BURA	MFG. APPO		AMPLIFIER			
AT'L:			SCALE			
	No. 7			DWG. A-4305	7.2	
		30	64	CODE	OF S	
			The second secon			





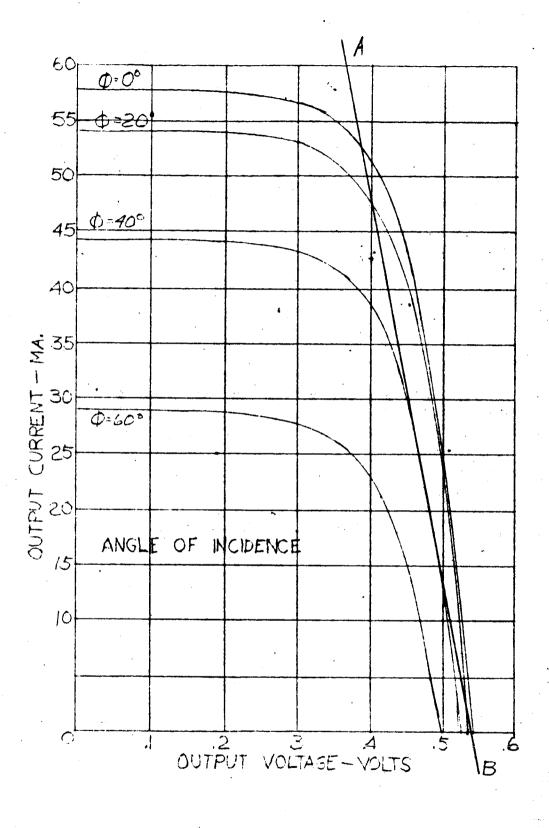
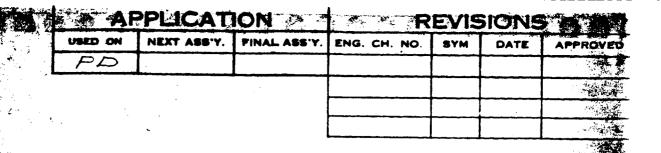
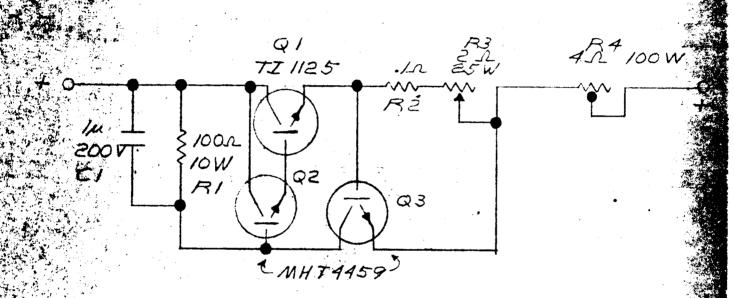


FIG. 25 TYPICAL SOLAR 67 CELL CURVES

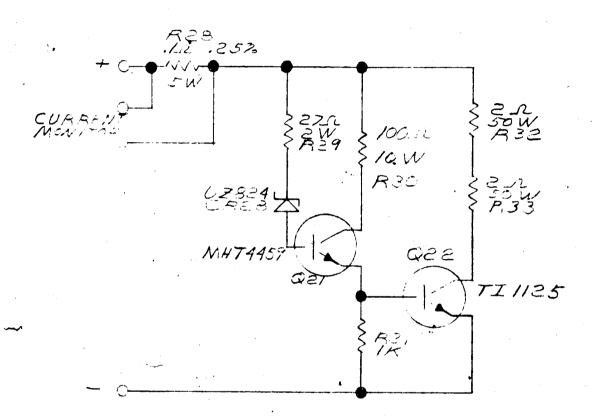




F16.26

ONLESS OTHERWISE NOTED	D9.	DATE			4	
MENSIONS ARE IN INCHES	CHK.		WWWX RESEARCH AND DEVELOPMENT CORP.			
AMBLES 2 1/64	ENG. APPD		TITLE	•		
e Duces	MFS. APPO		SOLAR PANE	L SIMULATOR		
MT A		·	SCALE			
				DWG. A-4309		
			. 68	CODE	OF	

USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVE
PD						



F16. 27

UNLESS OTHERWISE NOTED	OR.	DATE			学的方面
IMENSIONS ARE IN INCHES DLERANCES DEC. ± .008	CHK.		Marix RESEA	RCH AND DEVELOPMENT CORP	
FRAC. ± 1/64 ANGLES ± 1/4°	ENG. APPD		TITLE		
EBURR	MFG. AP®D		DETTERY.	SIMULATOR	
IAT'L:			SCALE	DWG. A 17/0	
	· ·		69	DWG. A-43/0	
an and the same and the same of the same o		 			- -

* A	PPLICAT	ION TO	THE PARTY	EVIS	HONE	
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
PD						
						,
						. <i>3</i> 166

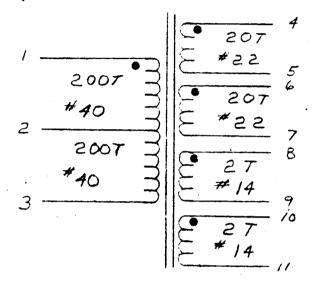
T,

CORE 80558-1F-240 RAYCHEM LEADS

MENSIONS ARE IN INCHES LERANCES DEC. ± .005 FRAG. ± 1/64	DR. DT	DATE 56	Matrix RESE	ARCH AND DEVELOPMENT CORP. NASHUA, NEW HAMPSHIES
ANGLES ± 1/4'	MFG. APPD		XT-621A	TRANSFORMER
			SCALE 71	DWe. A-4270

USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
PD						14.634
,						179504.194
						14:16 H
			•			James A.

Tz



CORE 52000-1F

F16,30

MENSIONS ARE IN INCHES	DR. OT	DATE /	A	
HERANCES	снк.		WOUNT RESEA	RCH AND DEVELOPMENT CORP.
DEC. \$\pm\$.008 FRAC. \$\pm\$.1/64 ANGLES \$\pm\$.1/4"	ENG. APPO		TITLE	
EBURR	MFG. APPD		XT 609B	TANNSFORMER
AT'L:				
			SCALE	owa. A- 4271
			72 ાલેક કર્યું છે.	CODE

*AI	PPLICAT	ION A	A R	EVE	SIONS	
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
PD				,		77.75
				Virian r	3	****
						W. Market
		-				200

73

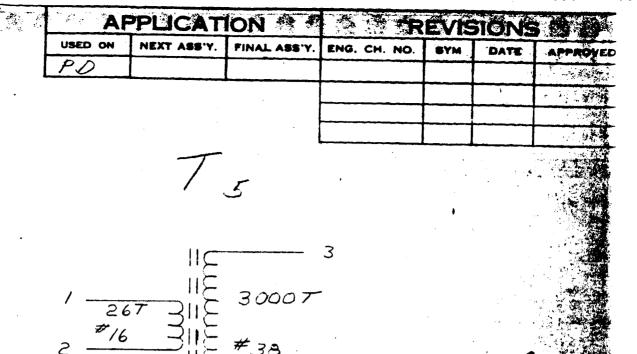
CORE 52000-1F.

UNLESS OTHERWISE NOTED	DR. DT	DATE >/66	M	
CLERANCES	сик.	1, 10	WWIX RESEA	ACH AND DEVELOPMENT CORP.
FRAC. ± 1/64 ANGLES ± 1/4'	ENG. APPO		TITLE	
IBURR AT'L:	MFG. APOD		XT625	TAANSFORMER
AI L:			SCALE	
				20° A-4272
		4.87.70 p	73	CODE

USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG.	CH. NO.	SYM	DATE	APPROVE
PD				·· · · · · · · · · · · · · · · · · · ·			
							. 22
							19
		•			<u> </u>	!	

FERROXCUBE CUP CORE
1811PLOD/3E
1811FID BODDING

UNLESS OTHERWISE IN IN DIMENSIONS ARE IN IN OLERANCES		DR. DT	DATE >/66	Matrix R	EBEARCH AND DEVELOPMENT CO	
FRAC. ±	.008 1/64 1/4	ENG. APPD		TITLE	NASHUA, NEW HAMPI	SHIRE S
HEURR		MFG. AP*D		XT 636	TRANSFORMER	
			 	SCALE	DWG. A- 4273	
The second secon				74	CODE	or



CORE 55202-AZ

JNLESS OTHERWISE NOTED	DR. 07.	DATE/66			100
IMENSIONS ARE IN INCHES PLERANCES DEC. TOOS	снк.	7 33	Wabux RE	SEARCH AND DEVELOPMENT C	ORP.
DEC. エ .008 FRAC. エ 1/64 ANGLES エ 1/4 ^c	ENG. APPD		TITLE	MASHUA, NEW HAMI	SHIME TO BE
ESURR	MFG. APPD		XTAOZ	TABNS FORMER	
AT'L:			SCALE	7 AMAS FOR MEA	
				DWG. A- 4274	
A STATE OF THE PROPERTY OF THE	Andrew Commencer of the second	and a Country of the second	ome the 75 or lake the same	CODE	OF TELES

4	A	PPLICAT	ION	TO REVISIONS 18				
	USED ON			ENG. CH. NO.		DATE	APPROVED	
	PD							
		,						
							_ 0	
	•						.5.4	

T 6

CORE 51/53-1F

UNLESS OTHERWISE NOTES		DATE /66	Matrix		
TOLERANCES DEC. ± .008 FRAC. ± 1/64 ANGLES ± 1/4	ENG. APPD		TITLE	ARCH AND DEVELOPMENT CORI	
DEBURR MAT'L:	MFG. APPD		XT619 T.	RANSFORMER	
			BCALE	DWG. A- 4275	
			76	coot	OF

<u> </u>	USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
Ĺ	PD	<u> </u>					
•							
					<u></u> j		
		7	>				

2.	/ .		
		2007	킈
		#38	3
BIFLERR	2		7
<i>017.244</i>	3	2007	
		#38	M.L
•	4	·	

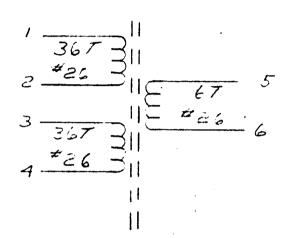
CORE 80558-11-240 RRYCHEM LENOS

Fig. 35

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN INCHES OLERANGES DEC. = .005	DR. DT	DATE 7/66	Matrix RESEARCH AND DEVELOPMS	ENT CORP.
FRAC. ± 1/64 ANGLES ± 1/4' DEBURR	ENG. APPD		XT 596A TAANSFORMS	
MAT'L:			SCALE DWG. A- 427	
			77	or a

USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
PD		•			-	
		:				*
						3

To



FERROX CUBE CUP CORE
1811PLOD/3E
1811FID BORDIN

F16:36

UNLESS OTHERWIS		DT DT	DATE //	A .		育
DIMENSIONS ARE IN OLERANCES DEC.		CHK.	1	Warix RESEA	ARCH AND DEVELOPMENT CORP.	
PRAC. ANGLES		ENG. APPD		TITLE	The state of the s	
EBURR		MFG. APPD		XT637 7	- AANS FOR MER	
1A1 C:				SCALE		
en e					88. A-4277	4.4
				78	CODE	P 6.3
			- 1 ° 4 1.±1.	e crisis de la compansión de la compansi	والأراف والمورية للماهدان والسيدان والمساعدة المطاردالمية	

	1 21071	O1 1 15 15 15	F	EVIS	こうころ	
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
PD	L					1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
	,					ुंद

T9

FERROXCUBE CUP CORE 1107PLOO 387 1107FID BOBBIN

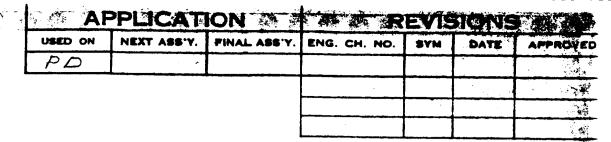
UNLESS OTHERWISE NOTED	DR. DT	DATE >/66	
DLERANCES	CHK,		WWW RESEARCH AND DEVELOPMENT CORP.
FRAC. ± 1/64 ANGLES ± 1/4	ENG. APPD		TITLE MARHUA, HEW HAMPSHIRE
EBURR	MFG. APPD		
AT'L:		·	XT638 TAANSFORMER
			SCALE 5000. A-42.78
		3 milk	79 CONT. 19

			THE TAX FAR		The state of the s	The state of the s
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVE
PD						
		,				
						1.3

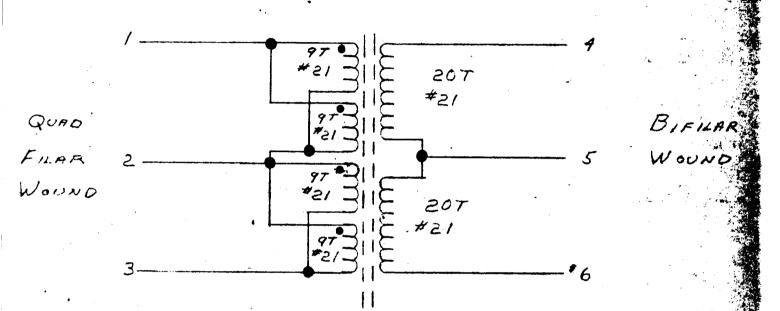
T10

CORE 52000-1F

					10.
UNLESS OTHERWISE NOTED	DR. 07	DAYE / 66			
IMENSIONS ARE IN INCHES	CHK.	1700	Matrix R	ESEARCH AND DEVELOPMENT COR	
DEC. ± .005		1		NASHUA, NEW HAMPSHII	
FRAC. ± 1/64 ANGLES ± 1/4'	ENG. APPD		TITLE		
EB URR	MFG. APPD		1		
AAT'L:			X7633.	TRANSFORMER	
		<u> </u>	SCALE	DWG. A- 4279	
		1		76.61	
			80	CODE	-
			<u> </u>	CODE	



TII



CUSTOM CORE MADE FROM CERMAG-24A PRODUCT OF STACKPOLE CARBON CO

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN INCHES FOLERANCES DEC. I.QUE	CHK.	7/66	Warix RESEARCH AND DEVELOPMENT CORP.
FRAC. ± 1/64 ANGLES ± 1/4	ENG. APPD	•	TITLE
SEBURR	MFG. APPD		XT639 ROTARY TARNS FORMER
			*** A-4380
			81 coes

A	PPLICAT	REVISIONS *					
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED	
PD							
·		:				¥	
		İ					

1.

607

CORE. 55926-A2

UNLESS OTHERWISE NOTED	DR. DT	7/65			
DIMENSIONS ARE IN INCHES	снк.		Worix RESE	ARCH AND DEVELOPMENT CORP	
DEC. ± .008 FRAC. ± 1/64 ANGLES ± 1/4	ENG. APPD		TITLE	NASHUA, NEW HAMPSHIRE	
ESURR	MFG. APPD		VTIOI		*
AAT'L:			X7626	CHOKE	ě
•			SCALE	DWG. A-4281	Ţ,
- Carlos Car			82	CODE /	> ,
	and the second of the second of		the second secon	the second of the control of the second of t	

A	PPLICAT	ION MY		EVIS	TONE	
USED ON			ENG. CH. NO.		DATE	APPROVED
PD						
						in the
						*

L2 & L6

16

CORE 55324-A2

INLESS OTHERWISE NOTED	_1	7/66	A		
LERANCES	CHK.		WWW RESE	ARCH AND DEVELOPMENT CO	
DEG. ± .008 FRAC. ± 1/64 ANGLES ± 1/4°	ENG. APPD	٠.,	TITLE		. A#
EURR	MFG. APPD		XT 634 C	~ HAKE	4
AT'L:	:		SCALE	2 MORE	
			BCALE	DWG. A-4282	10 July 10 Jul
	1	e Vo	83	CODE	of
		The second second second	TO A COLUMN TO SEC.	The second secon	

			R		IONS	
USED ON	NEXT ASS'Y.	PINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
PD						
						بنبوذ:
						. Olif

177 3|| *16 3||

CORE 55307-192

UNLESS OTHERWISE NOTED	DR. DT	DATE /66	M		
OLERANCES	снк.		WYWUX RESEA	ARCH AND DEVELOPMENT C	
DEC. ヹ.005 FRAC. ヹ1/64 ANGLES ヹ1/4*	ENG. APPD		TITLE		
DEBURK	MFG. APPD		XT628		
AAT'L:		<u> </u>		CHOKE	
			SCALE	DWG. A-4283	
Service Management II.	The second of th		84	CODE	OF IS

A A					MAKE	
DSED ON	NEXT ASS.Y. FINAL AS	18°Y.	ING, CH. NO.	WYB	PATE	APPROVED
PD		(1) (4) (4)				
		3	r .			
tan da sangaran san Sangaran sangaran sa			• 6			
		L			ı.	7. t.

FIG. 43

UNLESS OTHERWISE NOTED	DR. DT	DATE, 7/66	
OLERANCES A	CHK,		RESEARCH AND DEVELOPMENT CORP.
PRAC. © 1/64 ANGLES ± 1/4*	ENG. APPO	•	
EOUGH	MPS. APPD		
WY.		The state of	XT 631 CHOKE
			A-4284

A	PLICAT	ION		EVIS	SIONS	"被"解"
USED ON	NEXT ASS'Y.	FINAL ABS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED
PD					-	
						· · · · · · · · · · · · · · · · · · ·
						ूरी. जं
						4.

سى ك

25 T 3

CORE 55307-A2

F15.44

UNLESS OTHERWISE NOTED	DR. DT	2/66	A .	. •	
IMENSIONS ARE IN INCHES OLERANCES	CHK.	1		ARCH AND DEVELOPMENT CO	
PRAC. 2 1/64 ANGLES 2 1/4	ENG. APPD		TITLE	NASHUA, NEW HAMP	THINK .
COURR	MFG. APPD		·		
MT'L:			X7635	CHORE	
			SCALE	DWG. A-4285	
			86	CODE	OF

	I	I		
Eı	$(R_1 = 1K)$	$(R_1 = 2K)$		
1	195 ma	105 ma		
2	365 ma	205 ma		
. 3	525 ma	295 ma		
4	685 ma	380 ma		
5	840 ma	470 ma		

Test Data on Current Sample Circuit

Table 1

	$E_8 = 30V$		E = 20V		E _s = 10V	
E ₁	Duty Cycle	E	Duty Cycle	E,	Duty Cycle	Eo
.2V	9%	2.44V	8%	1.50V	8%	.59V
.5V	14%	3.98V	13%	2,54V	13%	1,12V
1.0V	23%	6.65V	22%	4.32V	22%	2:02V
1.5V	33%	9.43V	32%	6.18V	32%	2.97V
2.0V	42%	12.26V	42%	8.03V	41%	3.90V
3.0V	62%	17.88V	62%	11.82V	60%	5.80V
4.0V	82%	23.47V	81%	15.61V	80%	7.70V
5.0V	99%	29.13V	98%	19.35V	97%	9.60V

Test Data on Multiplier

Table 2

··	Manual Maximum	Controller Maximum
Eo	21.0 V	20.7V
I _o	605 ma	603 ma
Po	12.7 w	12.5 w
Es	36.1V	36.1V
Iin	955 ma	880 ma
Pg	34.5 w	31.8 w
Ein	16.2V	18.0V
Pin	15.5 w	15.8 w
Ep	22.3V	22.5V

Maximum Power Controller Test Data Manual vs Automatic Controlling

Table 3

	$R_{L} = 70.2\Omega$	$R_L = 34.3\Omega$	$R_L = 11.1\Omega$
I _{in}	875 ma	880 ma	865 ma
Eo	30.2V	20.7V	11.0V
I _o	430 ma	603 ma	990 ma
Po	13.0 w	12.5 w	10.9 w

Maximum Power Controller Test Data Output Power vs Load

Table 4

	-10°C	25°C	70 ° C	
Ein	38.72	38.36	38.55	volts
lin	2.773	2.794	2.788	amps
Pin	107.3	107.0	107.3	watts
Eo	23.71	23.70	23.68	volts
I _o	3.905	3,881	3.824	amps
Po	92.6	92.1	90.7	watts
n	86.2	86.0	84.5	efficiency %
Tc	.77	. 86	. 99	trickle charge (amps)

Final Test Data

Table 5

Power in (watts)	Power out (watts)	Efficiency %	Primary Turns 1/2 primary	Secondary Turns 1/2 Secondary
400	394.3	98.5	9	20
300	296.1	98.6	9	20
100	97.5	97.5	9	20
100	98.8	98.8	19	40

Transformer Characteristics: See Text

Table 6

9.

NEW TECHNOLOGY - The following two items are being reported under the New Technology clause:

1) A technique for maximizing the current from a variable voltage and/or resistance source into a dissipative load using a current transformer.

Ref: Matrix Memo 1966 POS1 Sec. 6.22, 7.0-7.8 and figs. 7 and 16 of this report

2) A voltage level detector circuit which is designed to detect a voltage level on the third terminal of a rechargeable Nickle Cadmium Cell.

Ref: Matrix Memo 1966 POS2 Sec. 7.9 and fig. 23 of this report CONCLUSIONS AND RECOMMENDATIONS - The major conclusion reached during this contract was that the use of a rotary power transformer and a maximum power sensing and controlling converter are practical for satellite power systems, as is evidenced by the breadboard delivered to NASA under the contract.

It is felt that the size, weight, and efficiency of such a system can be made compatible with spacecraft requirements. In actuality, the weight of a spacecraft power system could most likely be considerably reduced since more efficient use of the spacecraft's solar cells would allow a reduction in their number. This added efficiency could also allow a reduction in the amount of storage cells required in the spacecraft battery.

There appears to be no serious problem in increasing the power handling capability to higher levels (500 or 1000 watts). The breadboard, in fact, has been operated at a 320 watt level for a short period. Still higher power operation would require the use of higher current semiconductors and a slightly large transformer to accommodate the larger wire necessary to keep the wire losses down.

Other conclusions relating to the individual sub-systems of the non-dissipative charge controller using a rotary transformer are listed below:

- 1. A 2-transistor inverter using a center-tapped transformer can be designed to produce higher efficiency than a bridge type. This is discussed in the inverter section (6.1).
- 2. Synchronous rectification using SCR's is less efficient than the use of diode rectification followed by transistor pulsewidth switching.
- The simplest and most accurate method of achieving maximum power control was to maximize the current at the output of the system. This approach has two distinct advantages over the use of a circuit that maximizes the output of a power measuring circuit:
 - (a) There is less circuitry
 - (b) The operating tolerances required to obtain comparable

accuracy on the current maximizing circuitry are less than the requirements on the maximum power controller. The current maximizing approach, therefore, produces a smaller, lighter, and more reliable system than the power maximizing approach.

Based on the positive results of this contract, it is felt that a logical next step could be to increase the power level of the system to 500 or 1000 watts. Also, the design and fabrication of a prototype system employing both solar cells and batteries would be a valuable step in a more complete evaluation of the system.

11 BIBLIOGRAPHY

- 11.1 Prefiminary unpublished data from Stackpole Carbon Co. St. Marys, Pennsylvania, on CERMAG 24-B.
- 11.2 Specification sheet on HSP transistor #2N2877 and 2N2879 Honeywell Semiconductor Products, Riviera Beach, Florida
- 11.3 First Quarterly Report, Design and Development on a Non-dissipative Charge Controller
- 11.4 Second Quarterly Report, Design and Development of a Non-dissipative Charge Controler
- 11.5 TWX dated May 28, 1965
 Attn: Mr. Doug MacKinnon, Code 246
 Amendment of Matrix Proposal M2139P800 in response to
 RFP 636-38337-131
- 11.6 NASA contract NAS5-9204
- 11.7 Solar Cell Handbook International Rectifier Corporation
- 11.8 Permaloy Power Cores Catalog PC-303
 Magnetics, Inc., Butler, Pennsylvania
- 11.9 Design Manual featuring tape wound cores, catalog TWC-300, Magnetics, Inc., Butler, Pennsylvania
- 11.10 Ferroxcube Bulletin 330
 Ferroxcube Corporation of America, Saugerties, N. Y.
- 11.11 Engineering Notebook, No. 61
 Paul B. O'Sullivan
- 11.12 Engineering Notebook, No. 52
 LaVerne R. Philpott

12 GLOSSARY -

A Ampere

A_{co} Cross sectional area of the core

Ag Area of the air gap

Ap Peak amperes

A_{sh} Cross sectional area of the shell

AC Alternating current

Amp Ampere

AV Alternating Voltage

B Length of transformer winding

B See "Class B"

C Capacitor, Centigrade

Class B Operating mode of two transistors in push-pull connection in which only one transistor is conducting at a time, and for 180 electrical degrees.

Cm Centimeters

CR Diode

cosθ Power factor

d Diameter

DC Direct Current

DV Direct Voltage

Δ Increment

ΔV_{sh} Increased volume of ferrite shell

E Volts

Eb Battery voltage

Ebe Transistor base-to-emitter volts

Ebex Transistor base-emitter plus base external resistor volts

Ebextr Volts across the transistor base and external series resistor

Ebl Transistor base loss

Ece Volts between the collector and emitter of a transistor

Ei Supply volts

Esace Transistor saturated collector-to-emitter volts

F Operating frequency

FET Field effect transistor

Fm Magnetomotive force

H, Hz Hertz

h Efficiency

7: Inversion efficiency

I Current

Ib Transistor base current

Ibs Base current to saturate collector-emitter voltage

Ibsace Transistor base current to insure collector-to-emitter voltage with 50% margin

ID Ideal

Iex rms Exciting current in root mean square amperes

I_{ex} Exciting current

Ig Used with N as NIg to represent magnetizing force in the

air gap

Im Magnetizing current

in Inches

Iorms Transformer output root-mean-square current

L Primary current

Lpex Peak excitation current

Lpm Peak magnetizing current

Ipo Primary load current

Iprms Primary root-mean-square current

Is Secondary current

Isrms Secondary 2 root-mean-square current

J Jitter. Deliberate period perturbation

Rate of rise of excitation current

K (10)³ multiplier

K_{col} Specific core loss

Ko825 Ferrite loss constant at a flux density of 825 Gauss in

watt-sec per Hcm²

Kφ1345 Ferrite loss constant at a peak flux density of 1345 Gauss

in watt-sec per Hcm³

Kol Ferrite specific loss constant at any flux level

K_{shl} Specific shell loss

L Inductance

1 Length

Imcm Magnetic length in centimeters

amco Magnetic length of the core

1msh Magnetic length of the shell

1 mw. Magnetic effective length of the web

mv Millivolts

μ Magnetic permeability

μf Microfarad

Hop Magnetic permeability at the operating flux density

N Number of turns

Np Number of primary turns

N(40V) Primary turns when operating at 40V square wave at 10,000 Hertz

N(50V) Primary turns when operating at 50V square wave at 10,000 Hertz

NI Magnetizing force

NI_{cal} Ampere turns calculated

NI₀₀ Magnetizing force for the core

NI_{cow} Magnetizing force for the core and webbs of the trans-

NIg Magnetizing force to excite the air gaps

NI_{sh} Magnetizing force in the transformer shell

NIE Total magnetizing force

Degree

% Percent

P Power

P_{bl} Transistor base loss

P_{cl} Transistor collector loss

P_{col} Power loss in the core

P_{cow} Power loss in the core plus the end webbs

Pcow(50V) Core and webb loss at 50V supply

P_{culp} Copper losses in the transformer primary

Pculs Copper losses in the transformer secondary

Pexcul Excitation copper loss

Pexl Excitation loss

Pexl(40V) Excitation loss at 40V supply

Pexl(50V) Excitation loss at 50V supply

P_{fexl} Ferrite excitation loss

Pfl . Power loss in ferrite

Pg Total air gap exciting power

Pi Power in

Po Power out

Pgexl(40V) Air gap excitation loss at 40V supply

Pgexl(50V) Air gap excitation loss at 50V supply

P₁ Specific hysterisis power loss

P_{pcul} Primary copper loss

Presidual Loss constant for "Cermag" 24B in watts per cubic

centimeter Hertz

Pscul Secondary copper loss

P_{sh(50V)} Power losses in shell at 50V supply

P_{shi} Power loss in transformer shell

 P_{Σ} Total power

P_{Ecul(40V)} Total copper loss at 40V supply

PΣcul(50V) Total copper loss at 50V supply

P_{Σex}(40V) Total excitation losses at 40V supply

PΣf1(40V) Ferrite losses at 40V supply

Prf1(50V) . Total ferrite losses at 50V supply

Pn Total losses

P[1(40V) Total losses at 40V supply

PDI(50V) Total losses at 50V supply

PΣml Total active magnetizing losses

PΣQdl Total driving power per pair of transistors

PΣQ1 Total steady state transistor loss

PΣQ1(40V) Total transistor dissipation per pair at 40V DC supply

PΣQI(50V) Total transistor dissipation per pair at 50V DC supply

m Magnetic flux density

[©]co Magnetic flux density in the core

Peak magnetic flux density in the transformer shell

Peak total magnetic flux density

Φ_{CO} Total magnetic flux in the core

Q Transistor

R Resistor

Rb Internal resistance of battery

Rbextr Transistor base external resistor

RMS Root mean square

R_o Effective output load resistance

Rp Transformer primary winding resistance

RPT Rotary power transformer

R_s Transformer secondary resistance

Specific resistivity of copper at 60°C

S Switch

SCR Silicon controlled rectifier

²1(50V) Total losses with a 50V supply

Σ_{lm} Total magnetic losses

Total magnetic flux in the transformer core

T Transformer, turns ratio

Temperature

tg Length of the air gap

θ Phase angle of exciting current with respect to the impressed voltage

V Volts, volume

V₁₃₄₅ Ferrite volume in cm³ operating at α = 1345 Gauss

V_{co} Ferrite core volume in cm³

Vgow(40V) Volume of core and webbs operating with 40V supply

Vcow(50V) Volume of core and webbs operating with 50V supply

V_{sh} Volume of shell

Vsh(40V) Volume of shell operating at 40V supply

V_{sh(50V)} Volume of shell operating at 50V supply

V_w Volume of webbs

APPENDIX I

THE TEST TRANSFORMER (Rotary Transformer No. 1)

TEST TRANSFORMER - The first mechanical design excluded the problems of rotation and final support. The magnetic configuration, however, was chosen to permit rotation without perturbing the electrical characteristics. Two standard Ferroxcube ferrite cup cores as per Figure 45 were utilized. One was wound with 9 turns of litz wire (105 strands of #38 enamel wire), and the other with 8 turns. These were then bolted with a nylon bolt to form a nearly closed magnetic path. The winding in one cup was used as the primary, and the other as the secondary. The following data were measured or calculated:

Wire Characteristics

1. (DC resistance = AC resistance at 10KHz) = 0.00630 Ω/foot $\tau = 25^{\circ}\text{C}$.

- 2. Length for 9 turns = 17.7 inches for 8 turns = 15.7 inches
- 3. Resistance for 9 turns = $\frac{17.7}{12}$ (.00630) = .00938 Ω at 25°C.
- 4. Resistance for 8 turns = $\frac{15.7}{12}$ (.00630) = .00832 Ω at 25°C.
- 5. Resistance of wire at 65° C = .00718 Ω/foot
- 6. Resistance for 9 turns = $\frac{17.7}{12}$ (.00718) = .0106 Ω at 65°C.
- 7. Resistance for 8 turns = $\frac{15.7}{12}$ (.00718) = .00940 Ω at 65°C

Now the primary was wound with 9 turns and the secondary with 8.

Test Parameters

- 8. Output load resistance = 16Ω
- 9. Frequency (sinusoidal) = 10,000 Hz

·		Peak to Peak	. RMS
10.	Input volts	24.5	8.65
11.	Input amp	4.4	1.56
12.	Output volts	21.0	7.42
13.	Output amp	1.58	0.56

Calculations

- 14. Output watts = (7. 42 volts) (0.56 amp) = 4.50 watts
- 15. Power factor = output watts input voltamperes

$$\cos \theta = \frac{(14)}{4:5 \text{ watts}} = 0.3074$$

$$(10) \qquad (11)$$

16. Phase angle = cos⁻¹ .3074 = 72.10°. This assumes negligible internal losses. The worst actual case (still ignoring iron losses) would include the copper losses at high temperature, say 65°C.

From (6), (7), (11), and (13), we get the

17. Secondary copper losses = (output current)² (secondary resistance)

(13) (7)
$$P_{\text{culs}} = (0.56 \text{ amp})^2 (.0094 \Omega) = 0.0029 \text{ watts at } 65^{\circ}\text{C}$$

18. Primary copper losses = (input current) (primary resistance)

$$P_{\text{culp}} = (1.56 \text{ amp})^2 (0.0106 \Omega) = 0.0258 \text{ watts at } 65^{\circ}\text{C}$$

The actual power involved is

19.
$$P_{\Sigma}$$
 = Load power + secondary losses + primary losses

$$P_{\Sigma} = 4.50 \text{ watts} + 0.0029 \text{ watts} + 0.0258 \text{ watts}$$

= 4.53 watts

The actual power factor is more nearly

20.
$$\cos \theta = \frac{4.53 \text{ watts}}{(8.65 \text{ volts})(1.56 \text{ amps})} = 0.443$$
(10) (11)

and the phase angle is

21.
$$\theta = \cos^{-1} 0.443$$

= 63.79°

The magnetizing current is

22.
$$I_{m} = (Input current) \sin \theta$$

(11) (21) = (1.56 amp)
$$\sin \theta = 1.40$$
 amperes

With 9 turns on the primary, the magnetizing ampere turns were

Efficiency

Since this was excited with a sinusoidal waveform, the circulating magnetizing power is considered conservative and is found to be

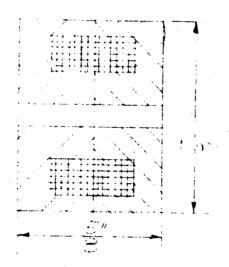
24. Exciting voltamperes = (Input volts) (magnetizing current)

This does not represent a power loss. Therefore the efficiency is

25.
$$h = \frac{\text{output power}}{\text{input power}} = \frac{4.50 \text{ watts}}{4.53 \text{ watts}} = 0.99^{-1}$$

This ignores iron losses. For these calculations, no figure of actual iron losses were available. Suppose, however, they would be equal to the copper losses, the efficiency would have been

26.
$$\frac{14}{4.50 \text{ watts}} = \frac{4.50 \text{ watts}}{4.50 \text{ watts} + 2(.0029 + .0258) \text{ watts}} = \frac{4.50}{4.56} = 0.987$$



7557 JEST JEST JEST S

APPENDIX I

THE MATHEMATICAL TRANSFORMER MODEL (Rotary Transformer No. 2)

MATHEMATICAL TRANSFORMER MODEL - The following design has taken into account the practical requirement of mechanical rotation and small bearing stiction. In principle this means that bearings should be small in diameter and lightly loaded. In the space environment, bearings are free from gravitational forces, and there remains only the magnetic moment with the earth's field, the electromagnetic air gap forces, electrostatic forces, maneuvering inertial forces, and forces due to strained secondary leads. Of these, the significant ones are considered to be the electromagnetic airgap forces and the strained wire forces. Inertial forces will be greater, but momentary. Air gap forces can be reduced to negligible proportions by balancing them, as in an arrangement in which all lines of force are normal to the axis of symmetry (radial). Edge fringing effects can be balanced also by having symmetrical shapes at each end of the transformer. Figure 46 illustrates the principle and is the design used for subsequent analysis along with Figure 47. The magnetic circuit is composed of a core 0.750" in diameter (d₄) with a 0.285" diameter hole (d₅). The net area is

27.
$$A_{co} = \frac{\pi}{4} (d_4^2 - d_8^2)$$

= $\frac{\pi}{4} (0.750 \text{ in})^2 - (0.285 \text{ in})^2$
= 0.380 in² $(2.54 \text{ cm})^2 = 2.45 \text{ cm}^2$

The outer diameter is 1.75" diameter (d₁). With the outer shell wall thickness of, say, 0.125", the outer diameter of the secondary coil will be 1.500". If half the window height is relegated to the primary winding and half to the secondary, and further if the magnetic circuit is broken by 2 air gaps which are coincident with the outer diameter of the primary (inner) coil, it would be at a diameter of

28. Diameter of air gap cylinder =
$$.750'' + (1.500'' - 0.750'')$$

$$d_{s} = 0.750 \text{ in } + \frac{(1.500 \text{ in } - 0.750 \text{ in})}{2}$$

$$= 1.125 \text{ in } \frac{(2.54 \text{ cm})}{1 \text{ in}} = 2.860 \text{ cm}.$$

For a trial calculation, let the air gap length be

29.
$$\tau_g = 0.004 \text{ in } \frac{(2.54 \text{ cm})}{1 \text{ in}} = 0.1015 \text{ cm}$$

Also, let the area be equal to the area of the core (see note at end of this section)

30.
$$A_g = 0.380 \text{ in}^2 \frac{(2.54 \text{ cm})^2}{1 \text{ in}^2} = 2.45 \text{ cm}^2$$

Since this is at 1.125" diameter, the axial length (thickness of the webb) will be

(27)
$$A_g = \pi d_3 l_2 = .380 \text{ in}^2 \left(\frac{2.54 \text{ cm}}{1 \text{ in}^2}\right)^2 = 2.45 \text{ cm}^2$$

or

$$l_2 = \frac{.380 \text{ in}^2}{1.125\pi \text{ in}} = .1075 \text{ in} \frac{(2.54 \text{ cm})}{1 \text{ in}} = 0.236 \text{ cm}$$

The shell thickness was set arbitrarily at 0.125 in for mechanical reasons. Its area will be larger than that of the core. It will be

32.
$$A_{sh} = \frac{\pi}{4} = \frac{(1.75 \text{ in})^2 - (1.50 \text{ in})^2}{4} = (3.063 - 2.250) \frac{\pi}{4}$$

$$A_{sh} = 0.640 \text{ in}^3 \frac{(2.54 \text{ cm})^3}{1 \text{ in}^3} = 3.99 \text{ cm}^3$$

From data furnished by the ferrite supplier (Biblio #1) the operating point was tentatively chosen, at which the following facts hold

33.
$$\infty$$
 = flux density = gauss = 1345 = arbitrary (from curves)

34. Material loss ("residual") = 2.8(10)-8
$$\frac{\text{watts}}{\text{Hcm}^3}$$
 = Km1345

For an operating frequency of 10,000 H, it is

35.
$$FK \approx 1345 = 2.8 (10)^{-3} \text{ watts/cm}^3$$

The value for loss above is almost constant in the vicinity of 10KH, varying directly as the square of the flux density.

36.
$$P_{\phi l} = 2.8 (10)^{-6} \frac{(\phi)^2}{1345} \frac{\text{watt-sec.}}{\text{H cm}^2} (\text{from curves})$$

37. Initial permeability
$$\mu_0 = 1200$$

Let the coil length be

38.
$$l_1 = 1.5 \text{ in } \frac{(2.54 \text{ cm})}{1 \text{ in}} = 3.81 \text{ cm}$$

The effective magnetic length of the shell or core is equal to the coil length plus the thickness of one end webb

(38) (31)
39. core mag length = (1.500 + .107) in
$$\approx$$
 1.61 in $\frac{(2.54 \text{ cm})}{1 \text{ in}}$
= 4.09 cm

If the outside diameter of the secondary coil is 1.500 in and the core diameter is 0.75 in, the magnetic effective length of each webb is

40.
$$l_{\text{mw}} = \frac{(38)}{1.500 \text{ in} - 0.750 \text{ in}}{2} + (.063 \text{ in} = 1/2 \text{ shell thickness})$$

$$+ (0.152 \text{ in} = 0.4 \text{ core radius}) = 0.590 \text{ in} \frac{(2.54 \text{ cm})}{1 \text{ in}}$$

$$= 1.50 \text{ cm}$$

The total magnetic length excluding the shell is

(39) (40)
41.
$$\Sigma_{lm} = 1.61 \text{ in} + 2 (0.590 \text{ in})$$

= 2.79 in $\frac{(2.54 \text{ cm})}{1 \text{ in}} = 7.10 \text{ cm}$

To evaluate the effect of magnetizing losses with different areas of air gaps, the ampere turns required for the circuit will be calculated. Ampere turns for a flux density of 1345 gauss for the core and webbs are developed first. Length units are centimeters.

42. NIcow
$$(4\pi) \mu_0 = \omega = 1345 \text{ gauss} = 1200 (4\pi) \text{ NIcow} \frac{1}{10} \frac{1}{10} \frac{1}{10} \frac{1}{10}$$

43. (NI)_{COW} =
$$\frac{1345(10)\text{lm}}{4\pi \, \mu_0} = \frac{3360}{\pi} \frac{(7.10)}{1200} = 6.32 \, \text{ampere turns}$$
(37)

The magnetizing force for the shell is

44.
$$NI_{sh} = 6.32 \frac{(2.45)}{3.99} \frac{(4.09)}{7.10} = 2.24 \text{ ampere turns}$$
(32) (41)

where

Let the airgap length be

45.
$$\tau_g = 0.004 \text{ in } \frac{(2.54 \text{ cm})}{1 \text{ in}} = 0.01015 \text{ cm}$$

With an area of A_g of 2.45 cm², (27), the airgap ratio without fringing effects is

46.
$$\frac{{}^{7}g}{{}^{4}g} = \frac{.01015 \text{ cm}}{2.45 \text{ cm}^{2}} = \frac{.00429}{\text{cm}}$$

So the magnetizing force is

47. NI_g = (1345 gauss)
$$\frac{10}{4\pi}$$
 $\frac{.01015}{2.45}$ (2 gaps in series) (27)

 $NI_g = 4.42 (2) = 8.84$ ampere turns

Total magnetizing forces in ampere-turns is

17.40 17.40 ampere turns

The total flux threading the core is

49. Total flux = flux density X core area

(33) (27)
$$\Sigma \omega_{CO} = A_{CO} \, \omega_{CO} = 1345 \, \text{gauss} \, (2.45 \, \text{cm}^2) = 3295 \, \text{maxwells}$$

Square Wave Excitation Mode - The velts per turn which this can support at 10KHz is

50.
$$\frac{\text{Volts}}{\text{Turns}} = \frac{E}{Np} = \frac{2 \text{ frequency X } \Delta \text{ flux}}{10^6}$$

$$= \frac{(35)}{2(10,000) (3295) \text{ H maxwells}}}{10^6}$$

= 0.659 volts peak/turn

The number of turns required to support a battery voltage of 50 volts is

51.
$$N_p = \frac{50}{.659} = 76 \text{ turns}$$
(50)

The litz wire tentatively chosen is made up of 105 number 38 wire, polyurethane insulated, double nylon-wrapped. It winds with about 16 turns per linear inch. Three layers each with 24 turns could be tried. The coil length is 1.5", so the number of turns per layer are

$$\frac{52. \quad N_p}{\text{layer}} = \frac{1.500 \text{ in}}{.063 \text{ in}} = \frac{24 \text{ turns}}{\text{layer}}$$

For three layers

$$N_p = 3(24) = 72 \text{ turns}$$

This is sufficiently close to the 76 required in equation (51). With 72 turns, the peak magnetizing current is

54.
$$I_{pm} = \frac{NI_{pm}}{N} = \frac{(48)}{72.} = .242 A_{p}$$
(53)

All the energy stored in airgaps is virtually recovered, except for losses in transistors and diodes. This amounts to that portion of the required ampere turns to magnetize the airgap to the total, or

55.
$$\frac{\text{airgap magnetizing force}}{\text{total magnetizing force}} = \frac{(47)}{17.40} = .508$$

$$(48)$$

To account for residual losses here, estimate the percentage airgap energy recoverable to be 75%, then the real airgap losses would be

56.
$$P_g = total \ excitation \ power \frac{(airgap \ magnetizing \ power)}{total}$$

(1 - airgap efficiency)

$$P_g = \text{watts} = \frac{1}{2} (50 \text{ volts}) (.242 \text{ amp}) (0.508) (1 - .75) =$$
= .770 watts

From magnetizing vs induction (B-H) curves supplied by the manufacturer, the residual induction after the magnetizing force is removed falls to about 85% of the peak value for typical non-saturating levels.

The ferrite excitation losses similarly are

57.
$$P_{\text{fexl}} = \frac{1}{2}$$
 (51) (54) (48) (57. $P_{\text{fexl}} = \frac{1}{2}$ (50 volts) (.242 amp) (8.56 = ferrite NI) (.85 = K_{col}) (48)

= 2.53 watts

The total active magnetizing losses are

58.
$$P_{\Sigma m1} = 0.770 \text{ watts} + 2.53 \text{ watts} = 3.30 \text{ watts}$$
 (56) (57)

To this there must be added a so-called "residual" loss specified by the ferrite supplier as equal to

58(a)
$$P_{residual} = 2.8 (10)^s \frac{watts}{Hcm^3} = K_{pl 345}$$

The volume of that portion of the magnetic circuit operating at 1345 gauss is

(27) (39) (30) (40)
59.
$$V_{1345} = V_{co} + V_{w} = 10.00 \text{ cm}^{3} + 3.68 \text{ cm}^{3} = 13.68 \text{ cm}^{3}$$

The core loss at $Hz = (10)^4$

(34) (59)
60.
$$P_{cow} 2.8 (10)^{-8} 13.68 (H=10^4) = 0.38 watts$$

The shell operates at a lower density than the core because its cross sectional area is larger. The flux density is

61.
$$\varphi_{sh} = \frac{(33)}{1345} \frac{\text{core area gauss}}{\text{shell area}}$$

$$\varphi_{sh} = 1345 \frac{2.45}{3.99} \text{ gauss} = 825 \text{ gauss}$$
(27)

The residual losses are proportional to the square of the peak induction, or

62. Loss constant of shell =
$$K_{\odot 825} = 2.8 (10)^{-8}$$

$$\frac{(^{\circ}sh = 825)^{2}}{1345^{2}} \frac{watts}{H cm^{3}}$$

$$(^{\circ}sh = 825)^{2} \frac{watts}{H cm^{3}}$$

$$(^{\circ}sh = 825)^{2} \frac{watts}{H cm^{3}}$$

Shell losses then are

63.
$$P_{sh} = 1.06 (10)^{-8} (10)^4 (10)^4 (10)^4 (10)^4 = 0.172 \text{ watts}$$

Total ferrite losses are

64.
$$P_{f1}$$
 (50V) = $\sum_{partial losses = .38 + .172 = .552 watts}$

Copper losses associated with (58) will now be determined. Assume the exciting current waveform to be triangular, the rms value is

65.
$$I_{exrms} = I_{pm} \frac{1}{3} / 3 = .242 (.578) = .14$$

This times the primary resistance will give the accompanying copper loss.

The primary wire length is

66. R_p = average length of turn X no. turns X resistance

$$R_{p} = \frac{\pi}{12} \frac{(27) (28)}{(.750 + 1.125)} 72 (.00718) \text{ ohms}$$

= 0.127 ohms

The excitation copper loss is

(54) (65) (66)
67.
$$P_{\text{excul}} = I_{\text{exrms}}^2 R_p = (.242)^2 (.577)^2 0.127 = .0024 \text{ watts}$$

Non-recoverable excitation losses are

(56) (57) (60) (63) (67)
68.
$$P_{exl} = 0.770 + 2.53 + 0.490 + 0.172 + 0.002$$

 $= 3.71 \text{ watts}$

This represents the standby losses. Total full load losses will be based on a 100 watt load at 50 volts. The load current then is

69.
$$I_{\text{orms}} = \frac{\text{watts}}{\text{volts}} = \frac{100}{50} = 2 \text{ amperes}$$

With this added to the excitation current of 0.242 amperes, the rms value can be approximated by

70.
$$I_{exrms} \approx amp + \frac{1}{2} (0.242) amp = 2.121 amperes$$

Primary copper losses are

(70) (66)
71.
$$P_{\text{culp}} = (2.121)^3 (0.127) = 0.572 \text{ watts}$$

Without at this time setting the transformer ratio, the secondary losses will be higher than the primary by the ratio of resistance

72.
$$R_s = R_p = \frac{1.5 + 1.125}{0.75 + 1.125} = \frac{\text{average secondary diameter}}{\text{average primary diameter}}$$

$$= \frac{(66)}{1.875} = .178 \text{ ohms}$$

The secondary losses then would be

73.
$$P_{cul} = I_o^2 R_s = (2)^2$$
 .178 = .712 watts

Total losses would then be

(68) (71) (73)
74.
$$P_{\Sigma 1} = 3.71 + .572 + .712 = 5.054$$
 watts

The power inversion efficiency is

75.
$$rac{7}{i} = \frac{\text{output power}}{\text{input power}} = \frac{(69)}{100} = .95$$
(69)

Equation (75) includes losses which are not dissipated within the transformer, and are properly associated with the total immediate conversion process. For instance, the power for the excitation current is derived from the supply volts and is considered largely lost. Outside of the actual copper and iron losses, this energy is spent in diodes and transistors.

- 76. Ferrite losses (from 64) = .552 watts
- 77. Copper losses (from 71 and 73) = 1,28 watts

78.
$$f_{\Sigma} = \frac{(69) (76) (77)}{100 (69)} \approx 0.98$$

Circuit Considerations - The choice of the basic operating voltage for the solar panel configuration depends primarily upon the availability of suitable transistors which can perform the necessary conversion and control functions. For 100 watt operation and with a stipulated 50V as the highest permissible choice, the current would be of the order of 2 amperes. Circuit efficiency is to be considered first for the first DC to AC inverter which permits the power to be transmitted through the rotary transformer. For the order of magnitude of current indicated above, the power lost in the switching transistors from its saturated collector to emitter voltage is sizeable, and therefore should be kept to a minimum. This fact considered alone would indicate a 2-transistor inverter using a centertapped transformer primary. However, this requires one-half of the primary winding to be always idle, which results in a larger and lossier unit. It also imposes serious voltage burdens on the transistors, more than doubling their standoff requirements. It is true that commutating spike voltages can exceed the continuous maximum rating without detriment, if they are short enough, but it is not deemed expedient to build in this condition as a steady operating requirement. In looking over the field for a suitable transistor, a trial choice is the 2N2879, rated at 5 amperes, and a standoff voltage of 100. The current rating is more than adequate, but for a 50V supply, there is no margin for 2 x 50V + spikes.

79.
$$2(E_i = 50) + (20 - spikes)$$

> (100V = 2N2879 standoff voltage)

Let us say that a voltage of 40 be chosen so that there would be a 20V spike margin, which can be safely observed. The current required to deliver 100 watts from the panel would be

80. I = amperes =
$$\frac{\text{watts}}{\text{volts}}$$
 = $\frac{100}{40}$ = 2.5 amperes

From the operating curves for the 2N2879 transistor at 100°C, the collector-to-emitter saturation voltage for 2.5 amp collector current is

81. $E_{\text{sace}} = 0.33 \text{ volts}$

The collector loss per series transistor is

(81) (80)
82.
$$P_{cl} = E_c I_c = (0.33) (2.5) = 0.83 \text{ watts}$$

To drive this transistor requires at least

83.
$$I_{bs} = \frac{1}{10} I_{c} = \frac{2.5}{10} = .25 \text{ amperes}$$

To take care of temperature variations and perturbations of power current, a margin of say 50% is required to insure saturation at all times, so

84.
$$L_{\text{bsace}} = .25 \times \frac{150\%}{100\%} = .375 \text{ amperes}$$

The base-to-emitter voltage is

from published curves. The base loss then is

86.
$$P_{bl} = E_{be}I_b = (1)$$
 (.375) = .375 watts

The total transistor dissipation then, not counting spike or commutating losses is the sum of (82) and (86), or

87.
$$P_{\Sigma Q1} = 0.83 + 0.375 = 1.21 \text{ watts}$$

To drive the base and stabilize the current, a limiting resistor is required. Set a value for it arbitrarily and let it be

So, the voltage drop across it for a current of .375 amperes is

89.
$$E_{bextr} = E_{be}I_{b} = (1) (.375) = .375 \text{ volts}$$

The driving transformer winding voltage, therefore, must be

90. E_{bex} = transistor base voltage + resistor voltage

$$E_{bex} = 1 + .375 = 1.375 \text{ volts}$$

The total driving power per transistor pair is

91.
$$P_{\Sigma \text{Odl}} = (E_{\text{bex}}) (I_{\text{b}}) = (1.375) (.375) = 0.515 \text{ watts}$$

To refer this to primary power consumption, consider it to be generated by an oscillator with an efficiency of 85%, so

92. Primary power drain =
$$\frac{\text{output power}}{\text{efficiency}} = \frac{0.515}{0.80}$$

= 0.645 watts

Transistor losses for a 2Q configuration (2 power transistors using a center-tapped transformer at $E_i = 40V$) are

さるできるからはないとは 後 後 できる (本)

93.
$$P_{\Sigma O1} = 0.645 + 0.83 = 1.48 \text{ watts}$$

In a bridge circuit, the current traverses two series transistors so the Q losses are doubled and for the same supply of 40V would be

(93)
94.
$$2P_{\Sigma Q1(40V)}$$
 2 (1.48 watts) = 2.96 watts

However, for a bridge rectifier the voltage could be higher so the current drain from the solar panel would be 2 amperes instead of 2.5 amperes, and the new losses in the bridge inverter would approximate

95.
$$2P_{\Sigma Q(50V)} \approx (0.8 = \frac{2}{2.5})$$
 (94)
2.96 = 2.3 watts

As mentioned above, this is the steady state inter-switching loss estimate and does not include commutating or spiking losses.

Transformer changes required to accommodate the 2-transistor inverter result in a heavier and less efficient design. In the first place the primary turns have to be doubled, since only half are used in any half cycle. Secondly, the supply voltage must be lowered to prevent over-voltaging the transistors. This affects the number of turns in the primary and secondary, and also the length of the magnetic circuit. Thus its size and conversion efficiency are modified. These changes are calculated below:

For a supply of 40V, the number of primary turns required to support a square wave at 10,000 hertz are

96.
$$N = \frac{40}{.659} \approx 60 \text{ turns}$$
(50)

For 3 layers, this requires 20/turns/layer and the coil length is

(52)
97.
$$B = (.063) (1 + 20.3) = 1.34$$
"

This extra turn space allows for the stacking factor. For a center tapped winding of 60 turns per side, the core length must be twice this, or

(97)
98.
$$2B = 2(1.34 in) = 2.68 in$$

The new magnetizing forces are

99.
$$NI_{sh} = 2.24 \frac{(2.68)}{1.61} = 3.72 \text{ ampere-turns}$$
(39)

and

100.
$$NI_{cow} = 6.32 \frac{(3.556)}{2.473} = 9.20 \text{ ampere-turns}$$
(41)

Total NI is

(47) (99) (100)
101.
$$NI_{\Sigma} = 8.84 + 3.72 + 9.20 = 21.76$$
 ampere-turns

With 60 primary turns, the peak exciting current is

102.
$$I_{pex} = \frac{21.76}{60} = 0.362 \text{ amp}$$
(96)

The excitation losses with a 40V supply are

103.
$$P_{\Sigma ex(40V)} = 0.770 + \frac{(102)}{2} (80) (57)$$

 $P_{\Sigma ex(40V)} = 0.770 + \frac{0.362}{2} (40) (.85) = 6.96 \text{ watts}$

104.
$$\frac{N(40V)}{N(50V)} = \frac{60}{72} = .835$$
(53)

(66) (104)
105.
$$R_p = 0.127$$
 (.835) = 0.106 ohms

(72) (104)
106.
$$R_s = .178$$
 (.835) = 0.148 ohms

(80) (102)
107.
$$I_{prms} = 2.5 + 1/2 0.362 = 2.82$$
 amperes

109.
$$P_{pcul} = I_{prms}^2 R_p = (2.62)^2 (0.106) = .845 \text{ watts}$$

(108) (106)
110.
$$P_{scul} = I_{srms}^2 R_s = (2.5)^2 (0.148) = 0.925 \text{ watts}$$

(109) (110)
111.
$$P_{\Sigma cul(40V)} = 0.845 \text{ watts} + 0.925 \text{ watts} = 1.77 \text{ watts}$$

The copper losses for a 50V supply are

112.
$$P_{\Sigma \text{cul}(50\text{V})} = 0.572 \text{ watts} + 0.712 \text{ watts} = 1.28 \text{ watts}$$
(71) (73)

The increased copper loss at 40V is

113.
$$P_{\Sigma \text{cul}(40\text{V})} - P_{\Sigma \text{cul}(50\text{V})} = 1.77 \text{ watts} - 1.28 \text{ watts}$$

= 0.49 watts

The increase of transformer excitation losses at 40V is

114.
$$P_{exl(40V)} - P_{exl(50V)} = 6.96 \text{ watts} - 2.28 \text{ watts}$$

= 4.68 watts

The airgap losses are the same for each voltage

115.
$$P_{gexl(40V)} - P_{gexl(50V)} = 0$$

Ferrite losses at 40V supply are proportional to its volume for the same operating peak magnetic flux

116.
$$P_{\Sigma fl}(40V) = P_{cow}(50V) = \frac{(V_{cow}(40V))}{V_{cow}(50V)} +$$

+
$$P_{sh(50V)}$$
 $\frac{(V_{sh(40V)})}{V_{sh(50V)}}$ - (27) (31)

= 0.66 watts + 0.44 watts

= 1.10 watts

The losses of inversion at 40V and 2 transistors

117.
$$P_{\sum 1(40V)} = 6.96 \text{ watts} + 1.77 \text{ watts} + 1.48 \text{ watts} + 1.10 \text{ watts}$$

$$= 11.31 \text{ watts}$$

To obtain the inversion losses for the 50V bridge chopper configuration, it is necessary as before to collect the partial losses as

Transformer magnetizing losses Ferrite losses Copper losses Transistor losses

At 50V, the load current for 100 watts is 2 amp (69). The transformer magnetizing losses are

118.
$$P_{\Sigma m1} = 3.71 \text{ watts (68)}$$

119.
$$P_{\Sigma fl(50V)} = 0.552 \text{ watts (64)}$$

120.
$$P_{\Sigma cul(50V)} = 5.05 \text{ watts (74)}$$

121.
$$\frac{1}{2} P_{\Sigma Q1(50V)} = (E_{\text{sace}} = .31V)^2 (I_i = 2.12) + (E_{\text{bex}} = 1.30)$$

$$(I_b = 0.3) (\frac{1}{.8})$$

$$= 0.657 + 0.49 = 1.147$$
 watts

122.
$$P_{\Sigma Q1} = 2(1.147) = 2.294 \text{ watts (95)}$$

So,

123.
$$P_{\Sigma 1(50V)} = 3.71 \text{ watts} + 0.55 \text{ watts} + 5.05 \text{ watts} + (95) + 2.29 \text{ watts}$$

= 11, 60 watts

Comparing this loss with that of the 2-transistor inverter, they are sufficiently close to be insignificant, since commutating and spiking losses are not considered, and the rather large portion attributable to the non-recoverable magnetizing losses are admittedly pessimistic. The comparison is

Chopper	<u>h</u> .	Ep
4Q	.883	50 volts
2Q	.894	40 volts

The closeness of these figures indicates the necessity of setting up parallel trials which can be done easily on the preliminary circuit breadboard.

Figures 46 and 47 show a magnetic circuit slightly different from what is discussed. The airgap area is roughly 7 times the area of the one discussed in equation (31). The magnetizing force required to drive 2 of these gaps is listed in equation (47). This is roughly half of that required for the entire magnetic circuit for the bridge type inverter. The following discussion assumed the stored energy of the airgap to be largely recoverable as reflected in equation (56). If it is not, then the airgap losses will be 4 times the value of 0.770 watts, or

(56)
124.
$$4P_g = 4(0.770 \text{ watts})$$

= 2.980 watts

This would increase the losses in equation (123) from 11.71 watts to

(123)
125.
$$P_{\Sigma 1}(50V) = 11.60 \text{ watts} + (3P_g = 2.31) \text{ watts}$$

= 13.91 watts

and the efficiency would drop to

126.
$$p_{(50V)} = {}^{(125)}_{.86}$$

With the large airgap area, the magnetizing force would drop from 8.84 (47) ampere turns to 1.26 ampere turns. The resulting efficiency would be

Figure 48A is a typical representation of a sinusoidal voltage wave (1) with the current, which includes power and magnetizing components (2). In Figure 48B, the current is broken into real and imaginary components, with the power current (long dashed curve) in phase with the applied voltage (2) and the magnetizing current (short dashed curve) in quadrature (3).

For the square wave case, Figure 48C illustrates a possible situation. The circuit is shown in Figure 49. This is a rudimentary schematic which does not include any of the refinements of the power matching networks. The voltage E₈ supplies the transistors Q3 and Q4 which drive the rotary transformer T-2. E-1 supplies the saturating oscillator-exciter transistors Q1 and Q2 which cooperate with transformer T-1. This furnishes square waves in the 10KHz region.

Referring again to Figure 48C, the solid line (1) represents the voltage across the whole primary of T-2. The dotted line (2) shows the typical power current. The dashed line (3) shows an ideal core magnetizing current wave shape. An ideal core is one which has a constant permeability and zero hysteresis. Since the impressed wave form is square, the magnetizing current wave form is triangular, and in lagging time quadrature to the voltage. Thus at the beginning of each half cycle, the excitation current and the power current are in opposition. The algebraic sum of these must be positive, that is the power current must always be larger than the excitation current if the polarity on Q3 or Q4 is to be such as to be conducting. During this time, energy which has been stored in the magnetic core is being extracted, and so long as the above relationship exists, this is largely recovered and transferred to the load. In this respect, the circulating magnetizing power is not being completely lost.

The square wave case and the sine wave case are similar. cases differ, however, to the extent that in the sine wave case, the magnetizing current can be the larger of the two, since magnetizing power is conservative and simply surges back and forth between the power source and the transformer. The square wave case, on the other hand, differs in that it can be considered only a quasi-conservative system. In each half cycle, all the stored energy in the core must be supplied by the battery, and instead of this energy circulating between the core and the power source, it is dumped each half cycle into the load. The power efficiency is roughly the same, because what energy the core delivers to the load the source does not have to supply. The only restriction is that power current be larger than the instantaneous magnetizing current. If the reverse is true, then at the beginning of each half period, the current is completely interrupted in Q3 and Q4, and at this point any remaining energy in the core is dissipated as shock-excited damped waves in the self-inductance of the transformer and stray circuit capacitance.

Again in the practical case, the ferrite does not return all the energy which is stored in it. The effect is to add to the losses of the system by heating the core. The effect on the current is shown in Figure 48D. The dashed line (2) shows the magnetizing and load currents of 48C added. The dotted line (3) shows the effect of hysteresis. The magnetizing current drops more rapidly to zero in the first half of each half period, thus not returning all the stored energy. The energy required to magnetize the core in the opposite sense then comes from the power source. The net loss is measured by the area between the curves (2) and (3). These wave forms would exist with the circuit of Figure 49 with the switch SI closed so that current drawn from the source can pulsate without changing the applied voltage to the power amplifiers Q3 and Q4.

If the values of the primary inductance of T2 and the capacitance C1 are chosen to be in resonance at the operating frequency, and further to have sufficiently low individual reactances to permit 10 or more times the power current as the circulating tank current, then the system will operate with essentially sine waves on the transformer with S closed, even with square waves impressed on the bases of Q3 and Q4. Figure 50 shows the various wave forms involved with this mode

of operation. Figure 50A is the AV wave form across capacitor C1 (Figure 49), and the terminals of transformer T2. In Figure 50B, the solid line shows the instantaneous voltage across the collector-emitter terminals of the transistor Q3, and similarly the dashed line shows the voltage across Q4. This means that the voltage at the center tap of T2 will follow the well-known full wave rectified and unfiltered form consisting sequentially of the dashed line above the base line for one-half cycle, then the solid line for the next half cycle, then the dashed line again, etc. This wave form is also across LI working about EI as the supply volts. In this case, Ll should have high reactance at all significant harmonics of the operating frequency. When the voltage is rectified from the secondary, the efficiency for the sine wave operation will be the same as for the square wave configuration if choke L2 (Figure 49) is larger than the critical value. Figure 50C shows the base drive voltage for transistor Q3.

The second transformer had its windings arranged as in Figure 51. Coil A occupied half the primary window at one end, and Coil B occupied the remainder. Similarly Coils C and D occupied their respective ends of the secondary windows. Current in Coil A then did not flow in the space occupied by Coil B, so the magnetic flux from A had large stray values in Coil B. Uneven voltages then were induced in Coils C and D with current in Coil A or B. This resulted in excessive self-inductances and unpredictable spike voltages and spurious pulse excited resonant frequencies.

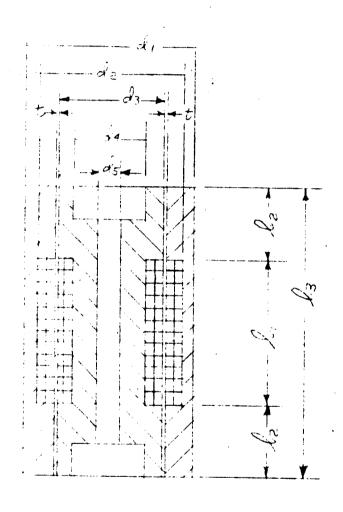
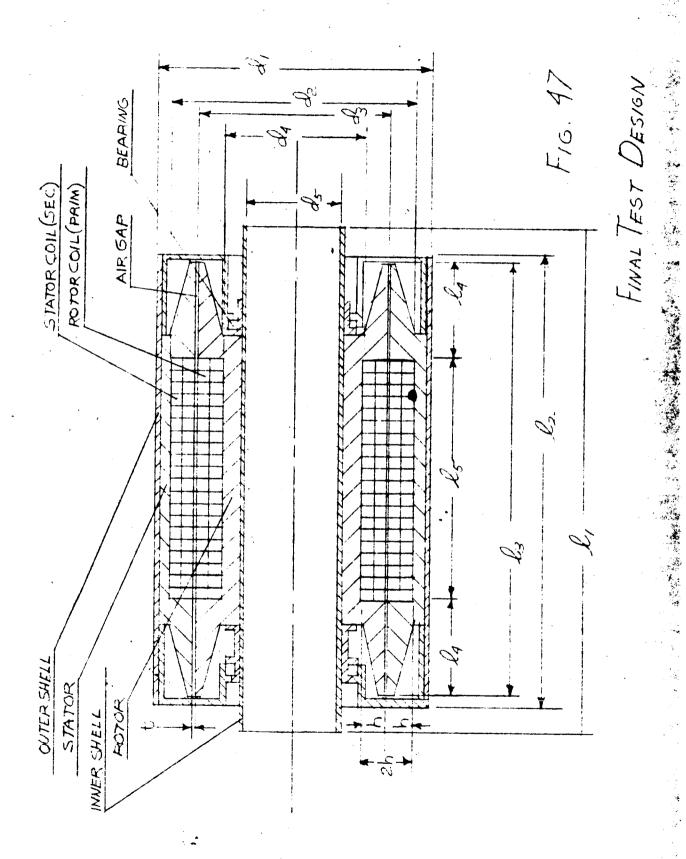
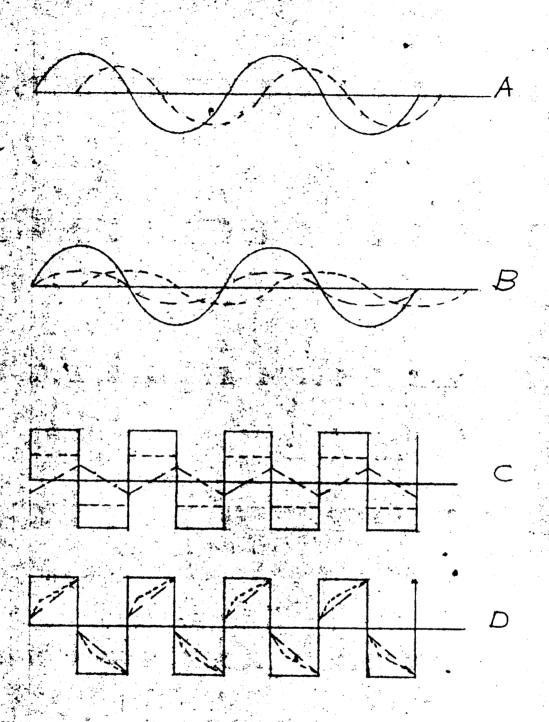


FIG. 46 MATHEMATICAL MODEL

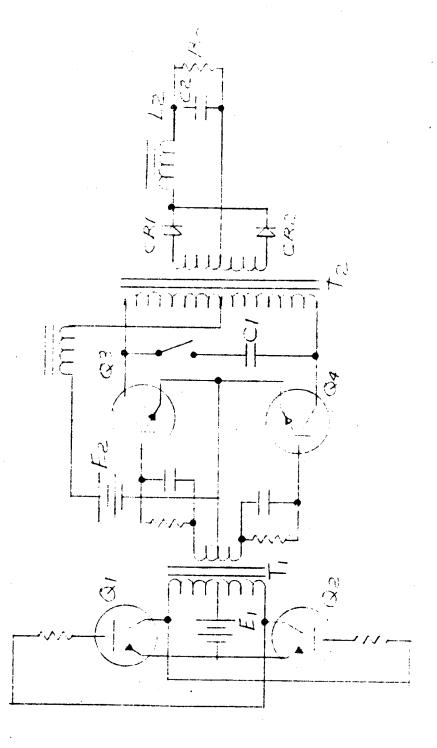


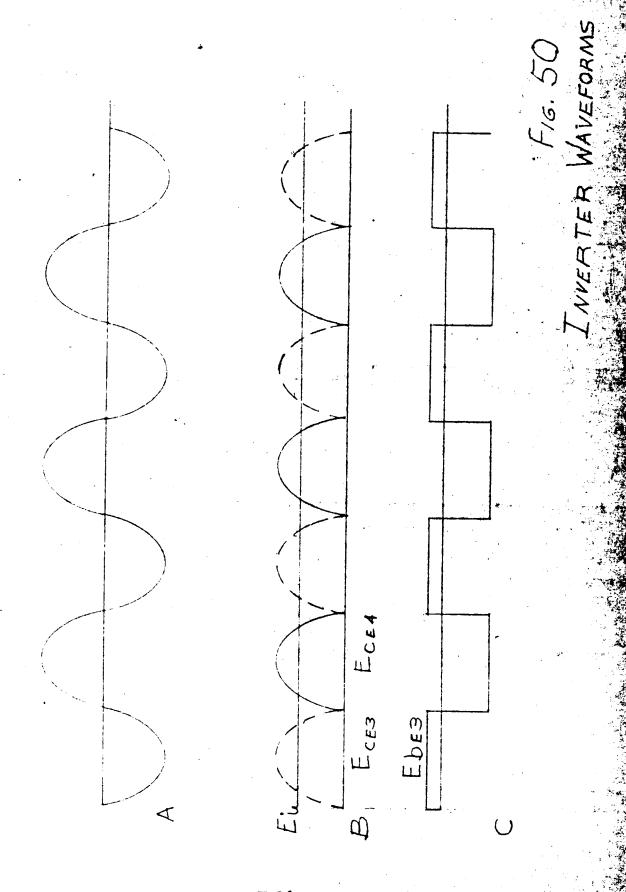
II-23



F16.48

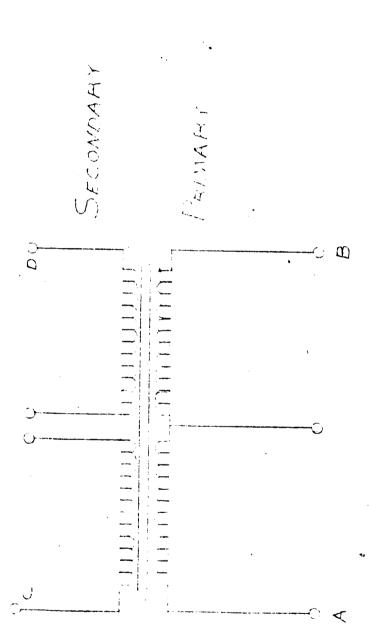
EXCITATION WAVEFORMS





II-26

F16. 51



APPENDIX III

REDESIGNED TRANSFORMER (Rotary Transformer No. 3)

REDESIGNED TRANSFORMER - The windings on this transformer are all wound with two conductors alongside, or bifilar. In this way all the current sheets generated by each winding occupy the entire coil volume, thus greatly increasing the primary-secondary coupling factor. Due to the limited winding space, all conductors were #19 B & S enamelled wire. The primary used two in parallel; the secondary one. The windings are summarized below:

Primary:

9 turns each side of center tap with two #19 wires in

parallel (bifilar wound)

Secondary:

20 turns each side of center tap with only one #19

wire (bifilar wound)

All winding windows were 1/8" high by 3/8" wide. The windings were wound and epoxy cast in molds without coil forms or spools. Figures 52 through 61 are detail drawings of the transformer basic components less terminal boards.

Magnetic Circuit Performance

In order to calculate this, it is necessary to determine the flux densities in the various parts. The maximum density in the core structure is in the inner cylinder, and in the shell assumed to be in the outer cylinder. First, the total flux required to support the primary voltage at the operating frequency will be determined.

Supply volts = 80V peak-to-peak = E Wave shape = square; symmetrical

Frequency = 10 KHz

Form factor of square wave to sine wave in determining peak flux density = $\frac{8}{7}$

The peak total flux required is

129. N = number of primary turns = 9, so

= 11.43 (10)³ Maxwells

The core density is Φ divided by the critical core area, or

130.
$$\alpha_{co} = \frac{\overline{\Phi}}{A_{co}}$$
 gauss

131.
$$A_{co} = \frac{\pi}{4} (D_8^2 - D_1^2)$$

$$= \frac{\pi}{4} [(1.5^{11})^2 - (1.125^{11})^2] \frac{6.45 \text{ cm}^2}{\text{in}^2}$$

$$= 5.25 \text{ cm}^2$$

and

132.
$$m_{co} = \frac{(129) (130) (131)}{11.43 (10)^8 \text{ Maxwells}}$$

$$= 2.18 (10)^3 \text{ gauss}$$

The specific losses due to hysterisis in this particular ferrite (Stackpole Cermag #24A) is stated by the manufacturer as about

133.
$$K_{01350} = 3.3(10)^{-6}$$
 f(cm³ = Volume) watts

at a density of 1350 gauss, and is proportional to the density squared, or

134.
$$K_{\odot 1} = \begin{bmatrix} \infty \\ 1350 \end{bmatrix}^2$$
 f (V) watts

The specific shell loss is then

135.
$$K_{shl} = \frac{(1.38)^2 \cdot 10^8}{(1350)^2} \cdot \frac{(133)}{3.3 \cdot (10)^{-8}}$$

$$= 3.47 \cdot (10)^{-8} \cdot \frac{\text{watts}}{\text{cm}^3 \cdot \text{Hz}}$$

Similarly, the specific core loss is

136.
$$K_{col} = \frac{(132)}{(2.18)^3} \frac{(133)}{(10)^5} = \frac{4.650}{1.820} 3.3 \frac{(10)^{-6}}{(10)^{-6}}$$

$$= 8.60 \frac{\text{watts}}{\text{cm}^3 \text{Hz}} \frac{(10)^{-6}}{(10)^{-6}}$$

The volume of the core ferrite is calculated next. From Figure 52, the volume is the sum of V_1 , V_2 , and V_8 .

Volume of the wedge cones ≈ (cross section) (average perimeter)

137.
$$V_1 \approx 2 \frac{1}{2} \frac{(1.750'' - 1.500'')}{2} \pi (\frac{1}{2} 1.75'' + 1.50'') (.355'')$$

$$(16.4) \frac{\text{cm}^3}{\text{in}^3}$$

$$= \frac{\pi}{4} (.250'') (3.25'') (.355'') 16.4 \frac{\text{cm}^3}{\text{in}^3}$$

$$= 3.72 \text{ cm}^3$$

Volume of two webbs =

138.
$$V_2 = 2 \frac{(1.750'' - 1.125'')}{2} \pi \frac{(1.750'' + 1.125'')}{2}$$
 (.188'')
$$(16.4) \frac{2m^3}{in^3}$$

$$= \frac{\pi}{2} (.625'') (2.875'') (.188'') 16.4 \frac{cm^3}{in^3}$$

$$= 8.70 \text{ cm}^3$$

Volume of cylinder is

139.
$$V_s = \frac{(1.50" - 1.125")}{2} \pi \frac{(1.50" + 1.125")}{2} (.375") 16.4 \frac{\text{cm}^3}{\text{in}^3}$$

$$= \frac{\pi}{4} (.375") (2.625") (.375") 16.4 \frac{\text{cm}^3}{\text{in}^3}$$

$$= 4.75 \text{ cm}^3$$

$$(137) (138) (139)$$

中國教徒 人名英格兰 医神经神经病病 中門在衛衛衛衛門

$$140. V_{co} = (3.72 + 8.70 + 4.75) cm^{3}$$
$$= 17.17 cm^{3}$$

Similarly, the volume of the shell ferrite is

141.
$$V_{sh} = 22.41 \text{ cm}^3$$

Now the ferrite losses can be determined by multiplying the ferrite volumes by the respective loss factors. For the core

(136) (140)
142.
$$P_{col} = K_{col}V_{cof} = (8.60) (17.17) (10)^{-6} (10)^{4}$$

= 1.475 watts

For the shell

The total ferrite losses then are the sum of (142) and (143)

144.
$$P_{\text{fexl}} = 1.475 + .776$$

= 2.25 watts

Copper Losses

The primary is wound with 9 turns of 2 strands of #19 wire in parallel. The copper resistivity is

145.
$$R_p = \rho \frac{1}{A}$$

146.
$$\rho$$
 = .6777 (1 + .014) 10⁻⁶ ohm-inches at 60°C = .688 (10)⁻⁶ ohm-inches

147. 1 =
$$N\pi \left(\frac{D_1 + D_2}{2}\right)$$

= $\frac{9\pi}{2}$ (1.750 + 1.500) inches
= 31.8 inches

Since there are two wires in parallel,

148. A =
$$\frac{2x\pi d^2}{4} = \frac{2x\pi}{4} (.0359)^2 = (2) .00101 in^2 = .00202 in^2$$

So that

149.
$$R_p = \frac{(146) \quad (147)}{6.88 (10)^{-7} (31.8) (10)^{+3}}$$

$$\frac{2.02}{(148)}$$

= 0.0108 ohms

The secondary likewise is

150.
$$R_g = \frac{\rho 1}{\frac{\pi d^3}{4}}$$

$$= (1.875) (\pi) (6.88) (10)^{-7} (20) (10)^{+3}$$

=
$$2.58\pi \ 10^{-3} = .0258\pi \ \text{ohm}$$

= .080 ohms

The primary copper losses for 100 watts input and j5 amperes excitation (peak-to-peak; measured) and 5 amperes load current (also peak-to-peak) are

151.
$$P_{\text{culp}} = R_{\text{cop}} \int_{t=0}^{t=a} I^{s} dt = \frac{1}{3} R_{\text{cop}} I^{s}$$

$$I_{p} = I_{po} + t \left(\frac{dI_{ex}}{dt} = k \right)$$

where

152.
$$k = 5(10)^4$$
 amperes per second

154.
$$I_p^2 = I_{po}^2 + 2 I_{po}kt + k^2 t^8$$

Power lost in the winding then is

155.
$$P_{\text{culp}} = \frac{R}{a} \int_{0}^{a} r_{\text{p}}^{\text{d}t}$$

$$P_{\text{culp}} = 2(10)^4 R_p = \frac{1}{3}(25)(5)(10)^{-6} + (2.5)(5)(10)^4 25(10)^{-10} + \frac{1}{3}(25)(10)^6 125(10)^{-15}$$

where

$$a = 5(10)^{-8} sec.$$

156.
$$P_{\text{culp}} = 2(10)^4 R_p$$
 $31.25(10)^{-5} + 312.5(10)^{-6} + 1.04(10)^{-4}$
= 15.58 R_p = 15.58 (.0108)
= .168 watts

For the secondary there is no excitation current, so the power current (assuming 100% efficiency) would be:

さん 小変 変異を変更をなけれる

157.
$$I_s = I_p \frac{N_1}{N_2} amp$$

$$= 2.5 \frac{9}{20} amp$$

= 1.125 amperes = constant

Secondary losses are:

158.
$$P_{culs} = I_s^2 R_s$$
(150)
= $(1.125)^2 .080 = .101 \text{ watts}$

The total copper loss is the sum of the primary and secondary losses, or

159.
$$P_{\sum cu} = P_{culp} + P_{culs}$$

(156) (158)
= .168 + .101
= .269 watts

Adding this to the ferrite losses, the total losses are

160.
$$P_{\pm} = W_{F} + W_{cop} = 2.25 + 0.269$$

= 2.52 watts

With 100 watts in, the output would be

(160)
161.
$$P_0 = (100 - 2.52)$$
 watts - 97.48 watts

The efficiency is then

162.
$$f_{0} = \frac{W_{out}}{W_{in}} 100 = \frac{(161)}{97.48} (100) = 97.48\%$$

$$\approx 97.5\%$$

Note that the ratio of ferrite to copper losses is 8.4. for highest efficiency is obtained when the ratio is unity.

This transformer is really proportioned for higher power--try, say, 300 watts. The primary current is the sum of the power and excitation currents.

The primary power current is

163.
$$I_{po} = \frac{300}{40} = 7.5 \text{ amperes}$$

With the same excitation current, the primary copper loss is

164.
$$P_{\text{culp}} = 2(10)^6 (0.0108) \frac{(163)}{56.25} \frac{(155)}{(10)^{-6}} + 15 (5) (10)^6 25 (10)^{-16}$$

$$+ \frac{1}{3} (25) (10)^8 125 (10)^{-15}$$

$$= 2(10)^6 (0.0108) 280 (10)^{-5} + 150 (10)^{-6} + 1.04^{-6}$$

$$= 0.652 \text{ watts}$$

The secondary is similarly treated.

165.
$$I_s = \frac{(163)}{7.5} \frac{N_p}{N_s} = 7.5 \frac{9}{20} = 3.375$$

166.
$$P_{culs} = 3.375^{8} (0.08) = 0.91 \text{ watts}$$

The total copper loss is

(164) (166)

$$P_{\Sigma_{CH}} = 0.65 + 0.91 = 1.56 \text{ watts}$$

The transformer efficiency is now

168.
$$f$$
 = $\frac{\text{output power}}{\text{input power}} = \frac{300 - (2.25 + 1.56)}{300}$
= $\frac{296.1}{300} = 0.986$
= 98.6%

Further calculations show higher efficiency at higher powers, say at 400 watts

169.
$$I_{po} = 10 \text{ amperes}$$

At this current level, the average of the power current and the power plus the excitation current: can be used to calculate primary copper losses

170. Ip
$$\approx \frac{10+12.5}{2} = 11.25 \text{ amp (169) (150-151)}$$

Primary losses are

171.
$$P_{\text{culp}} = I_p^2 R_p = (126.6) (.0108) = 1.37 \text{ watts}$$

Secondary losses are

172.
$$P_{\text{culs}} = I_s^2 R_s = \frac{(169) \frac{(165)}{(9)}}{10} = 0.080 = 1.62 \text{ watts}$$

The total losses now are

173.
$$P_{\Sigma l} = P_{\text{culp}} + P_{\text{culs}} + P_{\text{fl}} = (1.37 + 1.62 + 2.25) \text{ watts}$$

= 5.68 watts

Efficiency is (173)
$$174. \qquad h = \frac{400 - 5.68}{400} = .985 = 98.5\%$$

Within the calculation errors, this transformer has a peak efficiency of 98.6% at about 300 watts. In order to reduce losses at the 100 watt level, flux densities must be reduced. As an example, by increasing the length of the unit by 3/8", the total number of turns can be doubled, thus reducing the flux by a factor of 2, and the excitation current by almost a factor of 4. Again assuming these ratios are sufficiently accurate for illustrative purposes, then the shell losses would be reduced from 0.776 watts to

175.
$$\frac{P_{shl}}{4} (1 + \Delta V_{sh}) = 0.194 \cdot (1 + 0.358) \text{ watts}$$

= 0.263 watts

 ΔV_{sh} represents the effect of increased length of the transformer. Core losses would be reduced from 2.25 watts to

176.
$$\frac{P_{col}}{4}(1 + \Delta V_{co}) = .37 (1 + 0.277)$$
 watts

= 0.471 watts

 ΔV_{CO} represents the effect of increased length of the transformer. The copper losses are affected also. The secondary copper losses are doubled because the same current traverses twice the copper length, so

The primary has more than half the excitation current. In the original case there were 9 turns and a measured peak excitation current of 2.5 amperes. This gives a magnetomotive force of

178.
$$F_{m} = 9 (2.5) = 22.5 \text{ ampere turns}$$

This is divided between the shell ferrite, the core ferrite, and two air gaps. Fringe effects are neglected.

The shell length is

179.
$$l_{msh} = 1.190'' = 3.02 cm$$

The core length is

180.
$$l_{mco} = 1.185'' = 3.01 cm$$

Airgap length (one gap only)

181.
$$t_g = 0.005'' = .0127 \text{ cm}$$

Airgap area

182.
$$A_g = 1.750 - (.500) \text{ in}^3$$

= 2.75 in³ = 17.75 cm³

Gap length-to-area ratio for 2 gaps in series is

183.
$$2\frac{tg}{A_g} = \frac{.01}{2.75} = 3.64(10)^{-3} \text{ in}^{-1}$$

The magnetomotive force per 1000 gauss is

184.
$$\frac{NI_g}{1000} = 1000 \frac{(10)}{4\pi} 3.64 (10)^{-3}$$

= 2.89 ampere turns

The flux density required in the gap is

185.
$$m_g = \frac{11.43 (10)^3 \text{ Maxwells}}{A_g} = \frac{11.43 (10)^3}{17.75}$$
= 645 gauss

The actual magnetomotive force required then is

The core magnetomotive force can be calculated now, along with the effective permeability.

The core magnetic length is

187.
$$I_{mco} = 3.01 \text{ cm}$$

The core flux density is

(132)
188.
$$\omega_{CO} = 2.18 (10)^8$$
 gauss

The core magnetomotive force is

189.
$$NI_{CO} = \frac{2.18 (10)^8}{\mu} \frac{(10)}{4\pi} \frac{(187)}{3.01} = \frac{5.23 (10)^8}{\mu}$$
 ampere turns

The shell magnetic length is

(179)
190.
$$I_{sh} = 3.02 \text{ cm}$$

And the flux density is

(135)
191.
$$\omega_{sh} = 1.38 (10)^{3} \text{ gauss}$$

The shell magnetomotive force is

192.
$$NI_{sh} = \frac{(135)}{1.38(10)^s} \frac{(10)}{4\pi} \frac{(179)}{3.02} = \frac{3.31(10)^s}{11}$$

From (150) (151) the magnetomotive force measured was

193.
$$NI_T = 2.5(9) = 22.5$$
 ampere turns

But the calculated required ampere turns are

Now this equals NIT

(193) (194)
195.
$$22.5\mu = 1.86\mu + 6.61 (10)^3$$

$$\frac{20.64\mu}{20.64} = \frac{6.61}{20.64} (10)^3$$

$$\mu = 320$$

The published value for μ is in the neighborhood of $\mu_{op} = 1600$. This This gives a discrepancy of $\frac{1600}{320}$ or 5 times. The magnetic circuits

are made up of fabricated parts cemented together.

An effective airgap always exists regardless of the care in lapping the joints. The particular ferrite was so frangible that several breaks occurred which could not be restored to the original condition. Since at least 6 of these joints exist, the resulting effective cumulative gaps consume the additional magnetomotive force. Should the material have been homogeneous and of claimed quality, the magnetomotive force would have been

196.
$$NI_{ID} = 1.86 + \frac{6.61}{1.6} = 6.03$$
 (195)

ID = ideal

handle to the second of the se

and the excitation peak current would have been

197.
$$I_{ID} = \frac{6.03}{N} = \frac{6.03}{9} = 0.67 \text{ amperes}$$

Returning now to the case of the excitation current in the primary having twice the present turns, the extra length of the core and shell would require 3% more magnetomotive force. Using μ = 320:

198. NI =
$$1.86 + 1.31 \frac{(5.23 + 1.38)}{320} 10^{8}$$
 (194)
= $1.86 + \frac{8.65}{320} (10)^{2}$
= $1.86 + 27.0 = 28.86$ ampere turns

The primary magnetizing current will be

199. I =
$$\frac{(198)}{28.86}$$
 = 1.6 amp

The primary copper loss for the 100 watt case is developed below.

200.
$$k_1 = 3.2(10)^4$$
 amperes per second = $\frac{dI}{dt}$

The primary losses will be

201.
$$P_{\text{culp}} = 2(10)^{4} 2(.0108) \frac{(153)}{(6.25)} \frac{(153)}{5(10)^{-6}} + (2.5) \frac{(153)}{(3.2)} \frac{(10)^{+4}}{(10.24)} \frac{(155)}{(10)^{-10}} + \frac{1}{3} \frac{(154)(155)}{(10.24)} \frac{(155)}{(10)^{-15}}$$

= 0.24 watts

The total copper losses are now

202.
$$P_{cul} = P_{culp} + P_{culs}$$

(201) (158)
= (.24) + 2(.101)
= 0.442 watts

Compare this with the ferrite losses of

203.
$$P_{fl} = .263 + .471$$

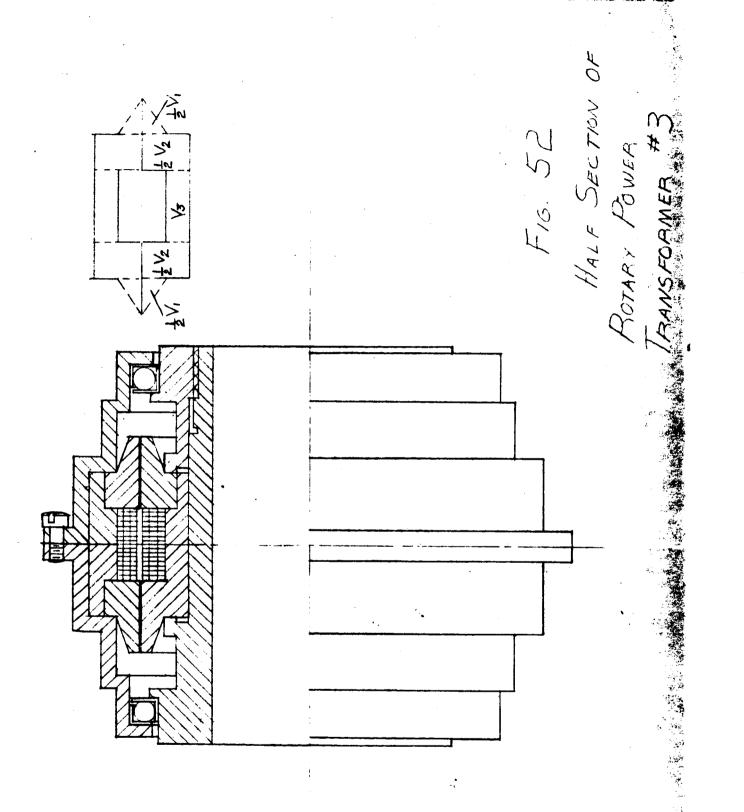
= 0.734 watts

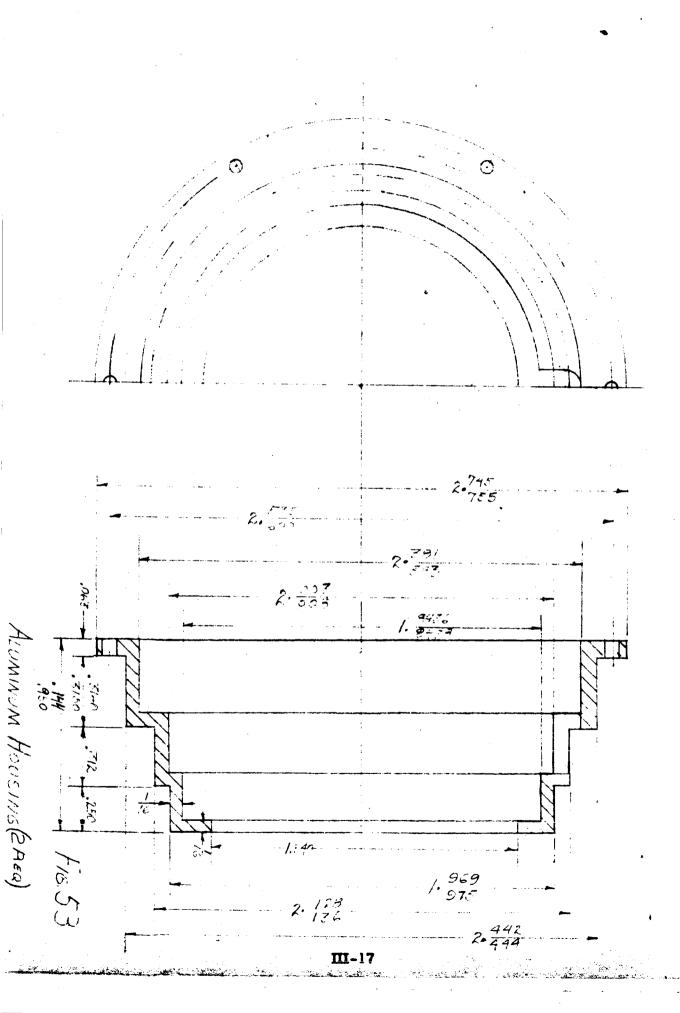
These are better matched for optimum*efficiency for its size. The efficiency is now

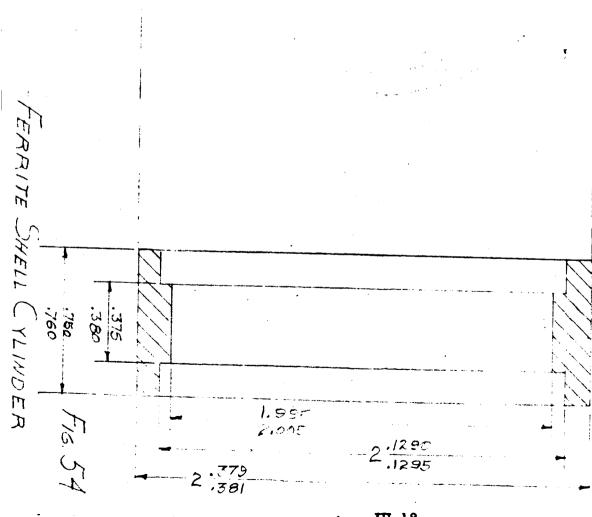
204. Total losses =
$$P_{\Sigma}$$
 = .442 .734
= 1.18 watts
(204)
205. $h = \frac{100 - 1.18}{100 - 1.18} = .988 = 98.8\%$

By increasing the length of the transformer 3/8" and doubling the number of turns on each winding, the efficiency is increased from 97.5% to 98.8%, or an increase of 1.3%.

The transformer characteristics are tabulated in Table 6.

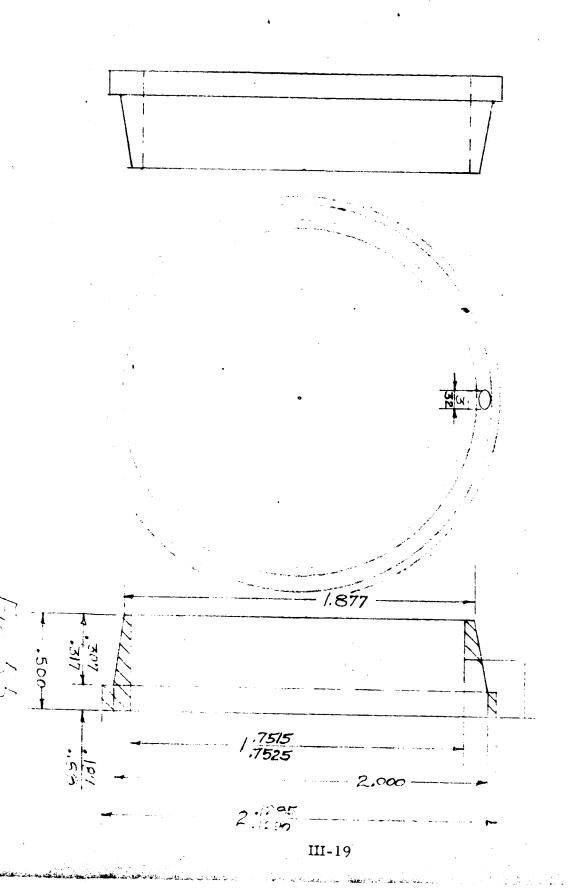


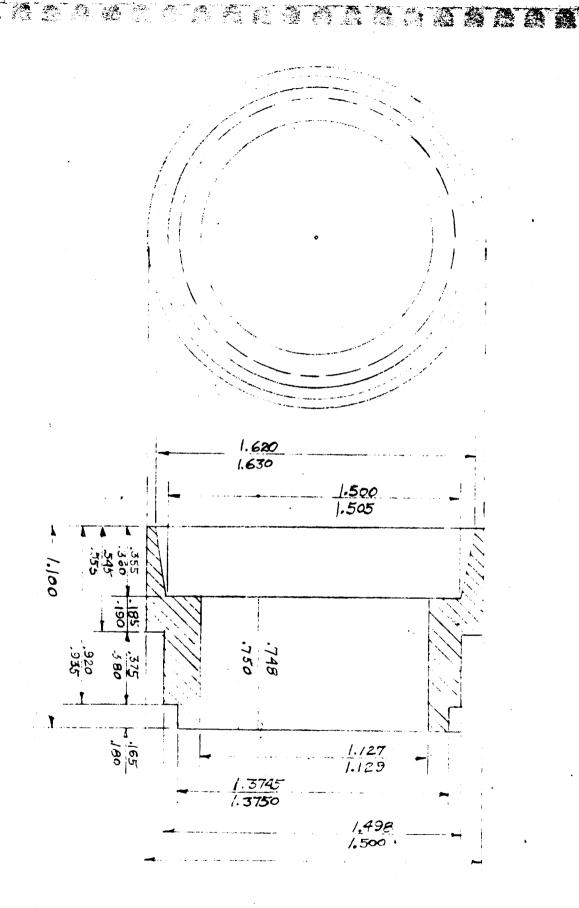




III-18

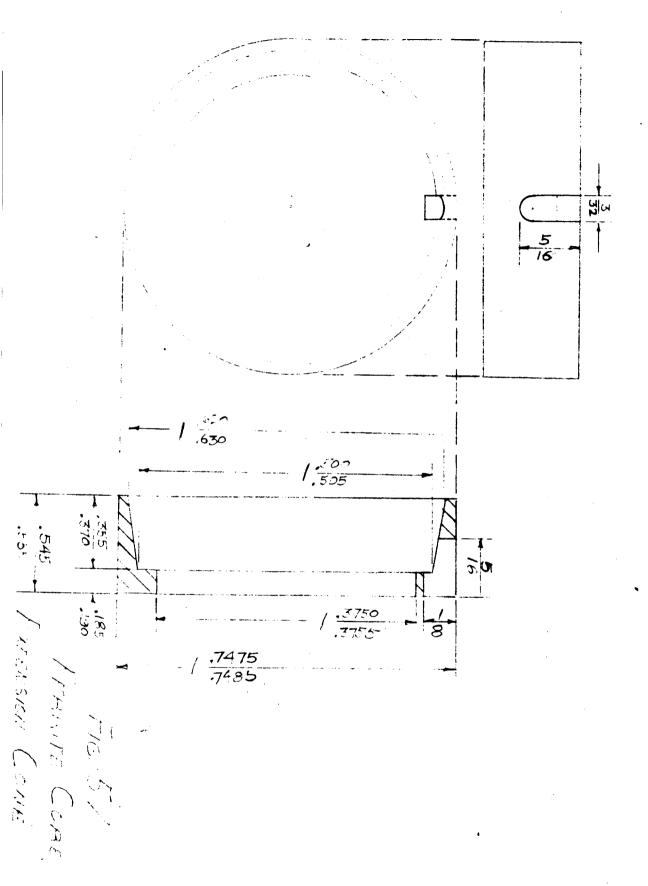
a can a con

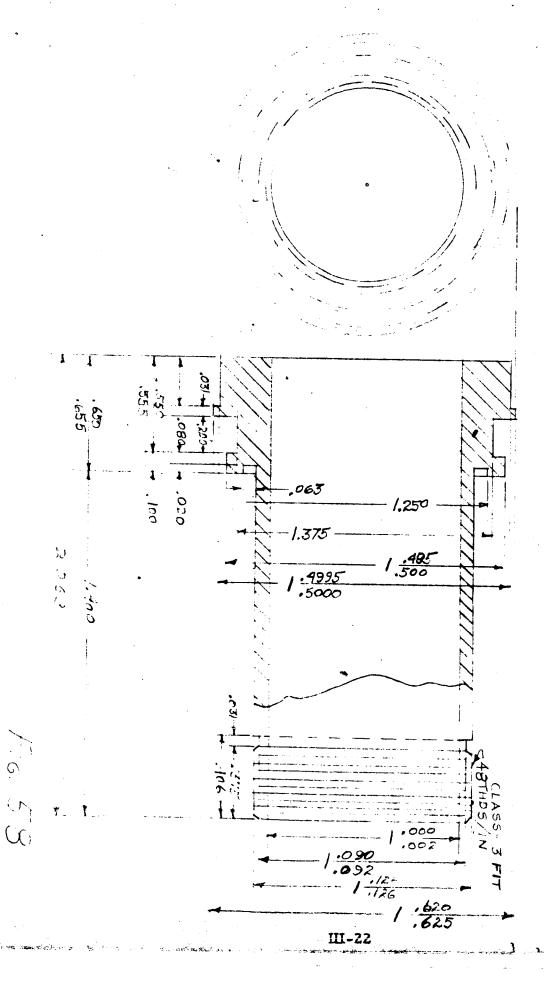




FERRITE COME

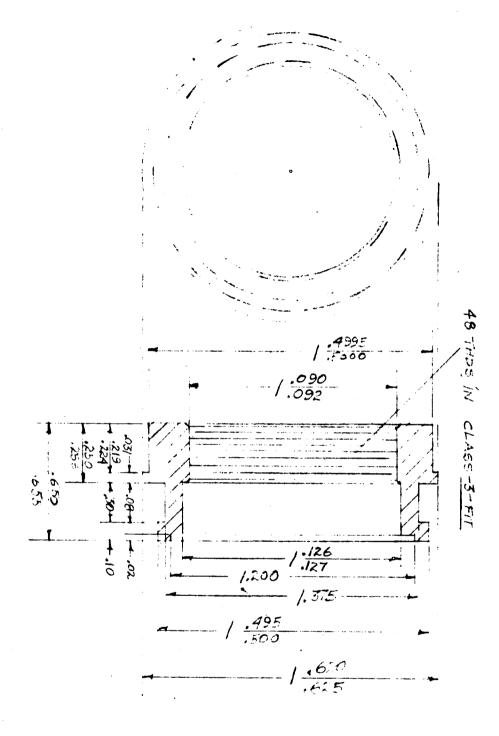
III-20





ALOMINON COTE ASSEMBLY QUILL

ALOMINUM QUILE NOT



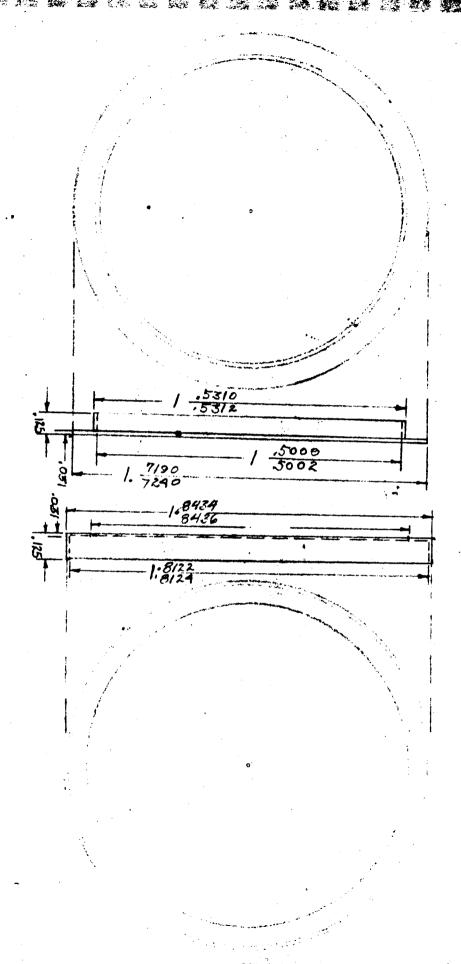
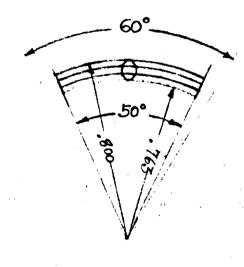
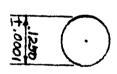


FIG. 60 BALLBEARING RACES



TEFLON SPACER &



APPENDIX IV

Maximum Power Conditions

MAXIMUM POWER CONDITIONS — One question that arose during the performance of this contract was what parameter should be maximized to obtain optimum operation. Should the solar array output power be maximized, should the power out of the rotary power controller be maximized, or should the battery current be maximized? Since the ultimate goal of the design is to provide the maximum usable power to the spacecraft, it appears that one of the last two choices is to be preferred. Further investigation, however, shows that the last two choices are equivalent maximum power out of the controller being equal to maximum current into the battery.

First, let us form a simplified model of the control system, Figure 62, . E_8 is considered the solar array generator, with R_{8a} being its internal resistance. R_C is the equivalent series resistance of the maximum power controller. For simplicity, R_{8a} and R_C are combined giving the total series resistance R_8 . E_b is the battery voltage, and R_b is the internal resistance of the battery. The connection between the source and the load is a pulse width regulator which we can consider to be a DC transformer. The input/output relationship of the DC transformer are E_1 = TE_8 and E_8 = TE_8 . The being the turns ratio of the transformer.

We are interested in the output power and current maximums as the transformer ratio (pulse width) is varied. First, let us find what value of T produces the highest output current (Is) by differentiating Is and setting the differential equal to zero.

206.
$$I_1 = \frac{E_8 - TE_b}{R_1 + TR_8}$$

207.
$$I_2 = TI_1 = \frac{E_8T - T^2E_b}{R_1 + TR_8}$$

208.
$$\frac{\delta I_{2}}{\delta T} = \frac{-R_{2} \quad E_{3} T^{3} - 2R_{1} E_{b} T + R_{1} E_{3}}{(R_{2} T^{2} + R_{1})^{3}}$$

Setting $\frac{\delta I_8}{\delta T}$ equal to 0 produces the following solutions for T

209.
$$T = \frac{-2R_1E_b + \sqrt{4R_1^2E_{b^2} + 4E_8^2R_1R_2}}{2E_8R_8}$$

210.
$$T = \frac{+}{2} \infty$$

Of the four solutions, only

$$T = \frac{-2R_1E_b - \sqrt{4R_1^2E_{b^2} + 4E_s^2R_1R_2}}{2E_sR_2}$$

is a maximum, and it also is the only solution which falls within the physical range of the DC transformer (pulse width regulator). The maximum power controller, when used as an output current maximizer, will therefore operate at this point.

Next, let us find the value of T, which produces the maximum output power. The output power arises from two terms, the power dissipated in the battery resistance (I_2 ² R_b), and the power which charges the battery (I_2 E_b). The total output power is therefore:

211.
$$P_0 = I_2^2 R_1 + I_2 E_b$$

212.
$$\delta P_0 = 2I_2 \left[\frac{\delta I_2}{\delta T} + \frac{\delta I_2}{\delta T} \right] E_b$$

$$= \left[\frac{\delta I_2}{\delta T} \right] (2I_2 + E_b) = 0$$

$$\frac{\delta \mathbf{I}_2}{\delta \mathbf{T}} = 0$$

214.
$$2 I_2 + E_b = 0$$

It is noticed that $\frac{\delta I_2}{\delta T} = 0$ is the same equation that we solved to find what

value of T produced an I₂ maximum. Also as before, the only term that produces a maximum and lies within the physical range of the DC transformer (pulse width regulator) is

215.
$$T = \frac{-2R_1E_b - \sqrt{4R_1^2E_{bs} + 4E_s^2R_1R_s}}{2E_sR_s}$$

a content to the content to the

Therefore, it can be concluded that maximum power into the battery and maximum current into the battery occur at the same point. Furthermore, if the power into the ideal battery Eb is maximized, it is noticed that it also occurs at the same value of T.

216.
$$P = I_2 E_b$$

217.
$$\delta P = \begin{bmatrix} \frac{\delta I_3}{\delta T} \end{bmatrix} E_b = 0$$

$$218. \qquad \frac{\delta I_2}{\delta \Gamma} = 0$$

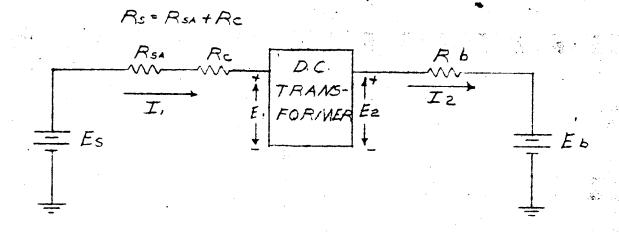
Therefore the choice between maximizing power and maximizing current becomes a question of the circuitry required to accomplish each technique. Since the current maximizing circuitry is less than that required for power maximization, the current maximizing approach was chosen for the breadboard. The proper operation of the current maximizing system, however, is not limited to a resistive or constant voltage load (battery), but will operate with any load for which E, I, and δE are positive in the operating range of the controller.

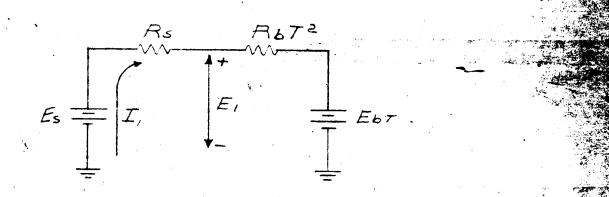
This can be demonstrated as follows:

219. If $\frac{\delta E}{\delta I}$ is always positive, then maximum I coincides with maximum E

220.
$$P = EI$$

If both E and I are maximums, then P must be a maximum. Therefore operating at the maximum output current is also operating at maximum power output.





F16 62

EQUIVALENT CKT FOR
MAXIMUM POWER CALCULATIONS